Sequential Circuits: Latches and Flip-Flops

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Thank John Wakerly for providing his slides and figures.
Sequential circuits

- Output depends on current input \textit{and} past history of inputs
- How can you tell an input is current or in the past?

- The circuits can \textit{remember} past inputs
  - “\textit{Memory}” is needed to remember the past

\[
\text{period} = t_{\text{per}} \\
\text{frequency} = 1 / t_{\text{per}} \\
\text{duty cycle} = t_H / t_{\text{per}}
\]
Bistable element

• The simplest sequential circuit
• Two states
  – One state variable, say, Q
Bistable element

- The simplest sequential circuit
- Two states
  - One state variable, say, $Q$

![Diagram of bistable element with inputs $V_{in1}$ and $V_{in2}$, outputs $V_{out1}$ and $V_{out2}$, and states LOW and HIGH]
Analog analysis

- Assume pure CMOS thresholds, 5 V rail
- Theoretical threshold center is 2.5 V
Analog analysis

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Analog analysis

- Assume pure CMOS thresholds, 5V rail
- Theoretical threshold center is 2.5 V

Metastable state
Metastability

- Metastability is inherent in any bistable circuit

\[ V_{\text{out}1} = V_{\text{in}2} \]

\[ V_{\text{in}1} = V_{\text{out}2} \]

- Two stable points, one metastable point

Transfer function:

\[ V_{\text{out}1} = T(V_{\text{in}1}) \]

\[ V_{\text{out}2} = T(V_{\text{in}2}) \]
Control bistable

- How to control it?
  - Control inputs S and R
- S-R latch

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>QN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>last Q</td>
<td>last QN</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
S-R latch operation

Metastability is possible if S and R are negated simultaneously.
S-R latch timing parameters

- Propagation delay
- Minimum pulse width

\[
\begin{align*}
S & \quad t_{PHL(SQ)} \\
R & \quad t_{PHL(RQ)} \\
Q & \quad t_{pw(min)}
\end{align*}
\]
S-R latch symbols

\[ \text{Diagram of S-R latch symbols} \]
S-R latch using NAND gates

<table>
<thead>
<tr>
<th>S_L</th>
<th>R_L</th>
<th>Q</th>
<th>QN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>last Q</td>
<td>last QN</td>
</tr>
</tbody>
</table>
## S-R latch with enable

Let C decide whether S and R can reach the bistable circuit.

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>C</th>
<th>Q</th>
<th>QN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>last Q</td>
<td>last QN</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>0</td>
<td>last Q</td>
<td>last QN</td>
</tr>
</tbody>
</table>

![S-R latch with enable circuit](image-url)
D latch

<table>
<thead>
<tr>
<th>C</th>
<th>D</th>
<th>Q</th>
<th>QN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>x</td>
<td>last Q</td>
<td>last QN</td>
</tr>
</tbody>
</table>

![D latch circuit diagram]
When \( C = 0 \), \( Q \) does not change.

When \( C = 1 \), \( Q = D \).
D-latch timing parameters

- When \( C = 1 \), \( Q \) follows \( D \)
  - Propagation delay (from \( C \) or \( D \))
- When \( C = 0 \), \( Q \) remembers \( D \)’s value at the \( 1 \to 0 \) transition
  - Setup time (\( D \) before \( C \)’s falling edge)
  - Hold time (\( D \) after \( C \)’s falling edge)
Positive edge-triggered D flip-flop

<table>
<thead>
<tr>
<th>CLK</th>
<th>CLK_L</th>
<th>Latch 1 Status</th>
<th>QM</th>
<th>Latch 2 Status</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>Disabled</td>
<td>$D_{prev} \uparrow$</td>
<td>Enabled</td>
<td>$Q_{M} = D_{prev} \uparrow$</td>
</tr>
<tr>
<td>↓</td>
<td>↑</td>
<td></td>
<td>$D_{prev} \uparrow$</td>
<td></td>
<td>$D_{prev} \uparrow$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Enabled</td>
<td>$\sim D$</td>
<td>Disabled</td>
<td>$D_{prev} \uparrow$</td>
</tr>
<tr>
<td>↑</td>
<td>↓</td>
<td></td>
<td>$D$</td>
<td></td>
<td>$D_{prev} \uparrow$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Disabled</td>
<td>$\uparrow D \uparrow$</td>
<td>Enabled</td>
<td>$Q_{M} = D \uparrow$</td>
</tr>
</tbody>
</table>
Positive edge-triggered D flip-flop behavior

<table>
<thead>
<tr>
<th>D</th>
<th>CLK</th>
<th>Q</th>
<th>QN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>x</td>
<td>0</td>
<td>last Q</td>
<td>last QN</td>
</tr>
<tr>
<td>x</td>
<td>1</td>
<td>last Q</td>
<td>last QN</td>
</tr>
</tbody>
</table>

![D Flip-flop schematic](image)
D flip-flop timing parameters

• Propagation delay (from CLK)
• Setup time (D before CLK)
• Hold time (D after CLK)
CMOS positive edge-triggered D flip-flop

- Two feedback loops (master and slave latches)
- Uses transmission gates in feedback loops
Positive edge-triggered D flip-flop with preset and clear

- Preset and clear inputs
  - Like S-R latch
Negative edge-triggered D flip-flop

- Invert the input CLK signal

\[ \begin{array}{cccc}
D & CLK_L & Q & QN \\
0 & 1 & 0 & 1 \\
1 & 1 & 1 & 0 \\
x & 0 & \text{last Q} & \text{last QN} \\
x & 1 & \text{last Q} & \text{last QN} \\
\end{array} \]
Positive-edge-triggered D flip-flop with enable

How does EN work?
Scan flip-flop

How is this circuit different from the previous one?

<table>
<thead>
<tr>
<th>TE</th>
<th>TI</th>
<th>D</th>
<th>CLK</th>
<th>Q</th>
<th>QN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>0</td>
<td></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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<td>1</td>
<td>1</td>
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<tr>
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<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>last Q</td>
<td>last QN</td>
</tr>
</tbody>
</table>
Scan flip-flops -- for testing

- TE = 0 → normal operation
- TE = 1 → test operation
  - All of the flip-flops are hooked together in a daisy chain from external test input TI.
  - Load up (“scan in”) a test pattern, do one normal operation, shift out (“scan out”) result on TO.
Edge-Triggered J-K flip-flop

- Not used much anymore
- Don’t worry about them

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>CLK</th>
<th>Q</th>
<th>QN</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>x</td>
<td>0</td>
<td>last Q</td>
<td>last QN</td>
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<tr>
<td>x</td>
<td>x</td>
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<tr>
<td>0</td>
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<td>last Q</td>
<td>last QN</td>
</tr>
<tr>
<td>0</td>
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<td>1</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>last QN</td>
<td>last Q</td>
<td></td>
</tr>
</tbody>
</table>
T flip-flops

\[ T \rightarrow Q \]

\[ Q \rightarrow Q \]

\[ T \rightarrow Q \]

\[ Q \rightarrow Q \]

\[ T \rightarrow Q \]

\[ Q \rightarrow Q \]

\[ T \rightarrow Q \]

\[ Q \rightarrow Q \]
T flip-flops with enable

- Important for counters
Many types of latches and flip-flops

- S-R latch
- S_L-R_L latch
- S-R latch with enable
- D latch
  - Edge-triggered D flip-flop
  - Edge-triggered D flip-flop with enable
  - Edge-triggered D flip-flop with preset and clear
- Scan flip-flop
- Edge-triggered J-K flip-flop
- Master/slave S-R flip-flop
- Master/slave J-K flip-flop
- T flip-flop
- T flip-flop with enable