Overview: Logic BIST

- Motivation
- *Built-in Logic Block Observer* (BILBO)
- *Test / clock systems*
- *Test / scan systems*
- *Circular self-test path* (CSTP) BIST
- Circuit initialization
- Test point insertion
- Summary
Motivation

- Complex systems with multiple chips demand elaborate logic BIST architectures
  - **BILBO** and *test / clock* system
    - Shorter test length, more BIST hardware
  - **STUMPS** & *test / scan* systems
    - Longer test length, less BIST hardware
  - **Circular Self-Test Path**
    - Lowest hardware, lower fault coverage
- Benefits: cheaper system test, Cost: more hardware.
- Must modify fully synthesized circuit for BIST to boost fault coverage
  - Initialization, *test point* hardware

Built-in Logic Block Observer (BILBO)

- Combined functionality of D flip-flop, *pattern generator, response compacter, & scan chain*
  - Reset all FFs to 0 by scanning in zeros
Example BILBO Usage

- **SI – Scan In**
- **SO – Scan Out**
- **Characteristic polynomial:** \(1 + x + \ldots + x^n\)
- **CUTs A and C:** BILBO1 is MISR, BILBO2 is LFSR
- **CUT B:** BILBO1 is LFSR, BILBO2 is MISR

(a) Example test configuration.

BILBO Serial Scan Mode

- **B1 B2 = \"00\"**
- **Dark lines show enabled data paths**
BILBO LFSR Pattern Generator Mode

- $B_1 \ B_2 = "01"$

BILBO in D FF (Normal) Mode

- $B_1 \ B_2 = "10"$
BILBO in MISR Mode

- \( B_1 \ B_2 = "11" \)

![BILBO in MISR Mode Diagram]

Test / Clock System Example

- New fault set tested every clock period
- Shortest possible pattern length
  - 10 million BIST vectors, 200 MHz test / clock
  - \( \text{Test Time} = \frac{10,000,000}{200 \times 10^6} = 0.05 \text{ s} \)
  - Shorter fault simulation time than test / scan

![Test / Clock System Example Diagram]
Test / Scan Systems

- STUMPS architecture
- Alternative test per scan systems
- Advantages and limitations of test/scan systems

STUMPS: Architecture and example

- $SR_1 \ldots SR_n$ – 25 full-scan chains, each 200 bits
- 500 chip outputs, need 25 bit MISR (not 5000 bits)
**STUMPS**

- **Test procedure:**
  1. Scan in patterns from LFSR into all scan chains (200 clocks)
  2. Switch to normal functional mode and clock 1 x with system clock
  3. Scan out chains into MISR (200 clocks) where test results are compacted
     - Overlap Steps 1 & 3

- **Requirements:**
  - Every system input is driven by a scan chain
  - Every system output is caught in a scan chain or drives another chip being sampled

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**Alternative Test / Scan Systems**

(a) Simple system.  
(b) Alternative system.
Test / Scan System

- New fault tested during 1 clock vector with a complete scan chain shift
- Significantly more time required per test than test / clock
  - **Advantage:** Judicious combination of scan chains and MISR reduces MISR bit width
  - **Disadvantage:** Much longer test pattern set length, causes fault simulation problems
- Input patterns – time shifted & repeated
  - Become *correlated* – reduces fault detection effectiveness
  - Use XOR network to phase shift & *decorrelate*

BILBO vs. STUMPS vs. ATE

- **LSSD:** *Level-sensitive scan design*
- **ATE rate:** 325 MHz  
  **System clock rate:** 1 GHz
- **P** = # patterns  
  **L** = max. scan chain length
- **CP** = *clock period* = $10^{-9}$ s
- **k** = \[ \frac{\text{Self-test speed}}{\text{LSSD tester speed}} \] = 3.07692

**Test times** – BILBO: \(P \times CP\)  
STUMPS: \(P \times L \times CP\)  
ATE: \(P \times L \times CP \times k\)

External test & ATE: 307 x longer than BILBO  
STUMPS: 100 x longer than BILBO
- Due to extra scan chain shifting
Circular Self-Test Path (CSTP) BIST

- Combine pattern generator and response compacter into a single device
- Use synthesized hardware flip-flops configured as a circular shift register
  - Non-linear mathematical BIST system
  - Superposition does not hold
  - Flip-flop self-test cell – XOR’s \( D \) with \( Q \) state from previous FF in CSTP chain
- MISR characteristic polynomial: \( f(x) = x^n + 1 \)
- Hard to compute fault coverage

CSTP System

(a) Single scanned flip-flop.
Examples of CSTP Systems

- CSTP BIST for 4 ASICs at Lucent Technologies:
  - Tested everything on 3 of the 4, except for:
    - Input/Output buffers and Input MUX
  - BIST overheads: logic – 20 %, chip area – 13 %
  - Stuck-at fault coverage – 92 %

Circuit Initialization

- Full-scan BIST – shift in scan chain seed before starting BIST
- Partial-scan BIST – critical to initialize all FFs before BIST starts
  - Otherwise we clock X’s into MISR and signature is not unique and not repeatable
- Discover initialization problems by:
  1. Modeling all BIST hardware
  2. Setting all FFs to X’s
  3. Running logic simulation of CUT with BIST hardware
Circuit Initialization (continued)

- If MISR finishes with BIST cycle with X's in signature, *Design-for-Testability* initialization hardware must be added
- Add *MS* (master set) or *MR* (master reset) lines on flip-flops and excite them before BIST starts
- Otherwise:
  1. Break all cycles of FF's
  2. Apply a partial BIST *synchronizing sequence* to initialize all FF's
  3. Turn on the MISR to compact the response

Isolation from System Inputs

- Must isolate BIST circuits and CUT from normal system inputs during test:
  - *Input MUX*
  - *Blocking gates* –
    - AND gate – apply 0 to 2^nd AND input, block normal system input
- Note: Neither all of the *Input MUX* nor the *blocking gate* hardware can be tested by BIST
  - Must test externally or with *Boundary Scan* (covered later)
Test Point Insertion

- BIST does not detect all faults:
  - Test patterns not rich enough to test all faults
- Modify circuit after synthesis to improve signal controllability
- Observability addition – Route internal signal to extra FF in MISR or XOR into existing FF in MISR

Summary

- Logic BIST system architecture --
  - Advantages:
    - Higher fault coverage
    - At-speed test
    - Less system test, field test & diagnosis cost
  - Disadvantage: Higher hardware cost
- Architectures: BILBO, test / clock, test / scan
- Needs DFT for initialization, and test points