Review

ISA: Instruction Specifications (for reference)

Instruction Specifications for the Simple computer - Part 1

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Opcode</th>
<th>Mnemonic Format</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increment</td>
<td>00000001</td>
<td>INC A</td>
<td>R[RA] = R[RA] + 1</td>
</tr>
</tbody>
</table>

Instruction Specifications for the Simple computer - Part 2

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Opcode</th>
<th>Mnemonic Format</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shift Left</td>
<td>00101110</td>
<td>SHR L</td>
<td>R[RA] = R[RA] SHL</td>
</tr>
<tr>
<td>Shift Right</td>
<td>00101110</td>
<td>SHR R</td>
<td>R[RA] = R[RA] SHR</td>
</tr>
<tr>
<td>Load Immediate</td>
<td>10101100</td>
<td>LD I</td>
<td>R[RA] = R[RB]</td>
</tr>
<tr>
<td>Add Immediate</td>
<td>10001010</td>
<td>ADD</td>
<td>R[RA] = R[RA] + R[RB]</td>
</tr>
<tr>
<td>Load</td>
<td>00100010</td>
<td>LD</td>
<td>R[RA] = R[RB]</td>
</tr>
<tr>
<td>Store</td>
<td>01000001</td>
<td>STA</td>
<td>R[RA] = R[RB]</td>
</tr>
<tr>
<td>Branch on Zero</td>
<td>11000001</td>
<td>BRZ</td>
<td>if (R[RA] = 0) then goto A</td>
</tr>
<tr>
<td>Branch on Negative</td>
<td>11000001</td>
<td>BRN</td>
<td>if (R[RA] &lt; 0) then goto A</td>
</tr>
<tr>
<td>Jump</td>
<td>11100000</td>
<td>JMP</td>
<td>R[RA] = R[RB]</td>
</tr>
</tbody>
</table>

State Table for 2-Cycle Instructions

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<tbody>
<tr>
<td>MOV A</td>
<td>00000000</td>
<td>MOV A</td>
<td>R[RA]</td>
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<tr>
<td>INC A</td>
<td>00000001</td>
<td>INC A</td>
<td>R[RA]</td>
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<tr>
<td>SUB A</td>
<td>00001010</td>
<td>SUB A</td>
<td>R[RA]</td>
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<tr>
<td>AND</td>
<td>00101000</td>
<td>AND</td>
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<tr>
<td>OR</td>
<td>00101100</td>
<td>OR</td>
<td>R[RA]</td>
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<td>XOR</td>
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<td>SHR L</td>
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<td>SHR R</td>
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<td>R[RA]</td>
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<td>LD I</td>
<td>10101100</td>
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<td>ADD</td>
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<td>STA</td>
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<tr>
<td>JMP</td>
<td>11100000</td>
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<td>R[RA]</td>
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Control Unit

Diagram of control unit and combinational register.
Final Exam

- May 6th (Tuesday), 10:30am-12:30pm, ITE 127
- Open-book, open-notes, and open-homework
- No cell phones, PDAs, or any other electronic devices except calculators
- Scope
  - Lectures 11-24
  - Homeworks 3-5
- Final project is due at 3pm on May 10 (FIRM)

Final Exam

- Topics
  - Sequential logic design
  - Finite State Machines, Storage/memory
  - Controller design – hardwired or micro-programmed (ASM)
  - VHDL coding
  - Pipelining
  - Floating point arithmetic

Final Exam – Focal Points

- ASM chart and description, conversion between ASM and FSM
- IEEE single-precision FP binary to decimal conversion
- Basic concept of pipelining, the five stages of a processor pipeline, the function of each stage
- Convert a non-pipelined datapath to pipelined datapath, analyze different timing requirements (consider register setup time, propagation delay of register and combinational circuits, hold time, the limit on circuit frequency)
- True/False questions: compare FPGA with custom VLSI design, pipelined latency and throughput, difference between simulatable and synthesizable design, SRAM/DRAM difference, etc.

Where do you go from here?

- Undergraduate study
  - Digital Design Lab (ECE4401)
  - VLSI Design (ECE3421)
  - Microprocessor Lab (ECE3411/CSE4903)
  - Computer Architecture (CSE 3666/CSE 4302)
  - Undergraduate Research Project
  - Senior Design

- Graduate study
  - Advanced VLSI design (ECE 6421)
  - VLSI CAD algorithms (ECE 6095)
  - Computer architecture
  - High performance computing
  - Computer security (GAANN fellowship)
  - Hardware Security and Trust
  - VLSI Design Verification and Test (ECE 6432)

- Jobs
  - Embedded design
    - Just about any industrial product manufacturer
    - From automobiles to toasters
    - Honeywell, BAE Systems, LMI, Toyota, GM, GE, etc.
  - High-performance chip design
    - Intel, IBM, AMD, Motorola
  - EDA
    - Cadence, Synopsys, Mentor Graphics
  - Aim high!

Where do you go from here?
Where do you go from here?

- Get more experience!!
  - Work with faculty
  - Get involved in more research
  - Try to work on larger projects
  - Take a couple of graduate courses
- Check out opencores.org
- Design your own boards
  - Development boards from
    - Xilinx
    - Digilent (www.digilentinc.com)
      - Excellent platform to allow you implement your ideas

VLSI Design Automation

- Large number of components
- Optimize requirements for higher performance
  - Performance relates to speed, power and size.
- Time to market competition
- Cost
  - Using computer makes it cheaper by reducing time-to-market.

VLSI Design Cycle

Layout

Semiconductor Processing

- How do we make a transistor?
- How do you control where the features get placed?
  - Photo lithography masks
Wafer Processing

Intel 4004
- First microprocessor
- Designed in 1971
- 2300 transistors
- 10-um process
- ~100 KHz

Intel Itanium Processor
- Released in 2005
- 1.72 Billion transistors
- 90-nm process
- 2 GHz

Testing Principle

ADVANCED Model T682 ATE
- Testers are very expensive ($150K – $20M)

GOOD LUCK!