Topics

- Performance Characterization
  - Interconnect Delay
  - Gate Delay
  - Switching Characteristics
Interconnect delay

• Lumped RC model

![RC Circuit Diagram]

- Charge $V_{in}$ to $V_{DD}$
- The transient output voltage is

$$V_{out}(t) = V_{DD} \left( 1 - e^{-\frac{t}{RC}} \right)$$

$$\frac{V_{DD}}{2} = V_{DD} \left( 1 - e^{-\frac{t_{dlh}}{RC}} \right)$$

$$\frac{t_{dlh}}{RC} = -\ln \left( \frac{1}{2} \right)$$

$$t_{dlh} \approx .69RC$$
Interconnect delay

• More accurate than lumped RC model
• More difficult to solve for large $N$
• Need full-scale SPICE simulation
Elmore Delay

- Single line model not useful for generalized RC tree networks
Elmore Delay

- First order calculation of time constant of the circuit

\[ t_d = \sum_{j=1}^{N} C_j \sum_{k \in \text{path}} R_k \]

\[ t_{d3} = R_1 C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + R_1 C_4 \]

\[ t_{d4} = R_1 C_1 + R_1 C_2 + R_1 C_3 + (R_1 + R_4)C_4 \]
Elmore Delay

\[ t_d = \sum_{j=1}^{N} C_j \sum_{k \in \text{path}} R_k \]

\[ t_{d3} = R_1(C_1 + C_2 + C_3 + C_4) + R_2(C_2 + C_3) + R_3C_3 \]

\[ t_{d4} = R_1(C_1 + C_2 + C_3 + C_4) + R_4C_4 \]
Elmore Delay

$$t_d = \sum_{j=1}^{N} \frac{C}{N} \sum_{k=1}^{j} \frac{R}{N}$$

$$= \frac{C}{N} \frac{R}{N} \frac{N(N+1)}{2} = RC \left( \frac{N+1}{2N} \right)$$

$$t_d = \frac{RC}{2} \text{ for } N \to \infty$$
Interconnect Delay

\[ t_d = 8\Omega \left( 20 \text{fF} + 10 \text{fF} \right) + 4\Omega \left( 10 \text{fF} \right) \]

\[ = 0.28 \text{ps} \]
Interconnect Delay

\[ t_d = 8\Omega \left( 20\ fF + 10\ fF + 10\ fF + 10\ fF \right) + 4\Omega \left( 10\ fF \right) \]

\[ = 0.44\ ps \]
Interconnect Delay

• Fanout Effects
  – Lines with multiple loads will have longer delays
    • Clocks
    • Data buses
    • Control lines
  – Solutions
    • Wider and thicker lines for special signals
    • Buffer drivers
Interconnect Delay

\[ t_d = \sum_{j=1}^{N} C \sum_{k=1}^{N} \frac{R}{N} \]

\[ = \frac{C \times R \times N \times (N + 1)}{N \times N} \times \frac{2}{2} = RC \left( \frac{N + 1}{2N} \right) \]

\[ t_d = \frac{RC}{2} \text{ for } N \rightarrow \infty \]
Interconnect Delay

\[ t_d = \frac{RC}{2} = \frac{1}{2} \left( r \frac{l}{w} \right) \left( c_a lw + c_p (l + w) \right) \approx \frac{1}{2} r c_a l^2 \]

- Delay is proportional to the square of the length
- Try to avoid long lines
Interconnect Delay

- Interconnect resistance
  \[ R = 0.07 \frac{5000\mu}{0.5\mu} = 700\Omega \]
- Interconnect capacitance
  \[ C_{\text{wire}} = 0.03 \cdot 5000\mu \cdot 0.5\mu + 0.044 \cdot 2 \cdot (5000\mu + 0.5\mu) = 515\ fF \]
- Intrinsic load capacitance
  \[ C_{\text{in}} \approx 5\ fF \]
- Propagation delay
  \[ t_p = \frac{RC_{\text{wire}}}{2} + RC_{\text{in}} = \frac{700 \cdot 515\ fF}{2} + 700 \cdot 5\ fF = 184\ ps \]
Interconnect Delay

- Avoid long interconnect delays using buffers

\[ R = 0.07 \times \frac{2500 \mu}{0.5 \mu} = 350 \Omega \]

- Interconnect capacitance

\[ C_{wire} = 0.03 \times 2500 \mu \times 0.5 \mu + 0.044 \times 2 \times (2500 \mu + 0.5 \mu) = 258 fF \]

- Intrinsic load capacitance

\[ C_{in} \approx 5 fF \]

- Propagation delay

\[ t_p = 2 \times \left( \frac{R C_{wire}}{2} + R C_{in} \right) = 2 \times \left( \frac{350 \times 258 fF}{2} + 350 \times 5 fF \right) = 94 ps \]
Interconnect Delay

- Avoid long interconnect delays using wider lines

\[ R = 0.07 \frac{5000 \mu}{5 \mu} = 70 \Omega \]

- Interconnect capacitance

\[ C_{wire} = 0.03 \cdot 5000 \mu \cdot 5 \mu + 0.044 \cdot 2 \cdot (5000 \mu + 5 \mu) = 1190 \ fF \]

- Intrinsic load capacitance

\[ C_{in} \approx 5 \ fF \]

- Propagation delay

\[ t_p = \frac{RC_{wire}}{2} + RC_{in} = \frac{70 \cdot 1190 \ fF}{2} + 70 \cdot 5 \ fF = 42 \ ps \]
Interconnect delay

• Interconnect sizing
  – Adjust delays
  – Prevent metal migration
  – Power supply noise and signal integrity
Interconnect Delay

- Directional Behavior

\[ t_d = 2\Omega(20\ fF + 10\ fF) + 4\Omega(10\ fF) \]
\[ = .10\ ps \]

\[ t_d = 4\Omega(10\ fF + 20\ fF) + 2\Omega(20\ fF) \]
\[ = .16\ ps \]
Switching Delay

- The intrinsic delay of a gate
- Transistor sizing can affect the delay
- Extrinsic capacitances can affect the delay
Delay Definitions

\[ \frac{V_{OH} + V_{OL}}{2} \]

\[ \frac{V_{OL}}{2} \]

\[ \frac{V_{OH} + V_{OL}}{2} \]

\[ V_{10\%} \]

\[ V_{90\%} \]

\[ t_f \]

\[ t_r \]

\[ t_{pHL} \]

\[ t_{pLH} \]
Switching Delay

- Fall time analysis

\[ V_{\text{out}} > V_{DD} - V_t \]

Saturated
Fall time analysis

- Saturated Mode

\[ I_C = I_{DS} \]

\[-C_L \frac{dV_{out}}{dt} = k_n \frac{(V_{DD} - V_{tn})^2}{2} \]

\[ dt = -2 \frac{C_L}{k_n (V_{DD} - V_{tn})^2} dV_{out} \]

\[ t_{f1} = 2 \frac{C_L}{k_n (V_{DD} - V_{tn})^2} \int_{V_{DD} - V_{tn}}^{9V_{DD}} dV_{out} \]

\[ t_{f1} = 2 \frac{C_L (V_{tn} - 1V_{DD})}{k_n (V_{DD} - V_{tn})^2} \]
Fall time analysis

- Linear Mode

\[
I_C = I_{DS}
\]

\[
-C_L \frac{dV_{out}}{dt} = k_n \left[ (V_{DD} - V_{tn})V_{out} - \frac{V_{out}^2}{2} \right]
\]

\[
dt = \frac{-2C_L}{k_n \left( 2(V_{DD} - V_{tn})V_{out} - V_{out}^2 \right)} dV_{out}
\]

\[
t_f^2 = \frac{-2C_L}{k_n} \int_{V_D}^{V_{DD}} \left( 2V_{out} (V_{DD} - V_{tn}) - V_{out}^2 \right) dV_{out}
\]
Fall time analysis

• Linear Mode

\[ t_f^2 = \frac{C_L}{k_n (V_{DD} - V_{tn})} \ln \left( \frac{V_{out}}{2(V_{DD} - V_{tn}) - V_{out}} \right) \frac{V_{DD} - V_{tn}}{V_{DD}} \]

\[ = \frac{C_L}{k_n (V_{DD} - V_{tn})} \ln \left( \frac{19V_{DD} - 20V_{tn}}{V_{DD}} \right) \]
Fall time analysis

\[ t_f = t_{f1} + t_{f2} \]

\[ = \frac{C_L}{k_n (V_{DD} - V_{in})} \left( \frac{2(V_{in} - .1V_{DD})}{V_{DD} - V_{in}} + \ln \left( \frac{19V_{DD} - 20V_{in}}{V_{DD}} \right) \right) \]

\[ = \frac{C_L}{k_n V_{DD}(1 - n)} \left( \frac{2(n - .1)}{1 - n} + \ln(19 - 20n) \right) \]

\[ n = \frac{V_{in}}{V_{DD}} \]

\[ K = \frac{1}{(1 - n)} \left( \frac{2(n - .1)}{1 - n} + \ln(19 - 20n) \right) \]

\[ t_f = K \frac{C_L}{k_n V_{DD}} \]
Fall time analysis

- Fall time is proportional to load capacitance and inversely proportional to $V_{DD}$ and $k_n$
- Decreasing the supply voltage will increase the fall time
- Increasing the transistor width will increase $k_n$ which will reduce the fall time
- Changing these three parameters can cause conflicting goals
Rise time analysis

\[ t_r = \frac{C_L}{k_p V_{DD}} \left( \frac{2(p - 0.1)}{1 - p} + \ln(19 - 20p) \right) \]

\[ K_p = \frac{1}{(1 - p) \left( \frac{2(p - 0.1)}{1 - p} + \ln(19 - 20p) \right)} \quad p = \frac{-V_{tp}}{V_{DD}} \]

\[ t_r = K_p \frac{C_L}{k_p V_{DD}} \]
Rise time analysis

- For equal fall times and rise times

\[
t_f = t_r
\]

\[
K_n \frac{C_L}{k_n V_{DD}} = K_p \frac{C_L}{k_p V_{DD}}
\]

\[
k_n = k_p
\]

\[
\mu_n C_{ox} \left( \frac{W_n}{L} \right) = \mu_p C_{ox} \left( \frac{W_p}{L} \right)
\]

\[
\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \approx 2 - 3
\]
Propagation Delay

• As with interconnect delay, find the equivalent resistance and load capacitance of the transistor

\[ t_{pHL} = 0.69 R_{eq} C_L \]
Propagation Delay

\[ R_{eq} = \text{average}(R_{on}(t)) = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_{DS}(t)} \]

- Propagation delay is the time for voltage to reach half way point - so integrate from \( V_{DD} \) to \( V_{DD}/2 \)

\[ R_{eq} = \frac{1}{V_{DD}/2 - V_{DD}} \int_{V_{DD}}^{V_{DD}/2} \frac{V_{DS}(t)}{I_{DS}(t)} dV_{DS} \]

- For the output range we are interested in, the transistor is always in saturation

\[ R_{eq} = \frac{-2}{V_{DD}} \int_{V_{DD}}^{V_{DD}/2} \frac{V_{DS}}{I_{DSAT}(1 + \lambda V_{DS})} dV_{DS} \]
Propagation Delay

\[ R_{eq} = \frac{-2}{V_{DD}} \int_{V_{DD}}^{V_{DD}/2} \frac{V_{DS}}{I_{DSAT}(1 + \lambda V_{DS})} dV_{DS} \]

\[ = \frac{2}{V_{DD} \lambda^2 I_{DSAT}} \left( \lambda V_{DS} - \ln(1 + \lambda V_{DS}) \right) \bigg|_{V_{DD}/2}^{V_{DD}} \]

\[ = \frac{2}{V_{DD} \lambda^2 I_{DSAT}} \left( \lambda V_{DS} - \left( \lambda V_{DS} - \frac{\lambda^2 V_{DS}^2}{2} + \frac{\lambda^3 V_{DS}^3}{3} - \cdots \right) \right) \bigg|_{V_{DD}/2}^{V_{DD}} \]

\[ = \frac{2}{V_{DD} I_{DSAT}} \left( \frac{V_{DS}^2}{2} - \frac{\lambda V_{DS}^3}{3} + \cdots \right) \bigg|_{V_{DD}/2}^{V_{DD}} \]

\[ = \frac{2}{V_{DD} I_{DSAT}} \left( \frac{3V_{DD}^2}{8} - \frac{7\lambda V_{DD}^3}{24} + \cdots \right) \]

\[ \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{7}{9} \lambda V_{DD} \right) \]
Propagation Delay

- Load capacitance
Propagation Delay

- Load capacitance
  - Intrinsic capacitance - sum of capacitances at drain - $C_{GD} + C_{DB}$
Propagation Delay

• Intrinsic Capacitance
  – $C_{GD}$ is composed solely of overlap capacitance
    • The transistors are either in cutoff or in saturation, so no channel capacitance exists
  – The actual load capacitance relative to ground is $2C_{GDO}$ because of Miller effect
Propagation Delay

\[ t_{PLH} = 0.69 R_{eq} \left( 2C_{GDOn} + 2C_{GDPo} + C_{DBn} + C_{DBp} + C_{ext} \right) \]

- Extrinsic capacitance is composed of wire capacitance and input capacitance of fanout
- Input capacitance is composed of overlap capacitance and channel capacitance
  - Overlap capacitance is \( C_{GDO} + C_{GSO} \). Miller effect is ignored because \( V_{out} \) is assumed to be constant
  - Channel capacitance is \( C_{ox}WL \). Assume worst case
- All capacitances are roughly proportional to \( W \)
- Equivalent resistance is inversely proportional to \( W \)
Next class

- Delay Analysis
- CMOS Logic Design
- Chapter 6.1 and 6.2