VLSI Design and Simulation

Lecture 4

CMOS Processing Technology
Topics

• CMOS Processing Technology
Semiconductor Processing

• How do we make a transistor?

• Fabrication Process
Wafer Processing

- Silicon single crystal growth from polysilicon
- Silicon ingot with impurities is created
- Ingot diameter can vary from 100mm to 300mm
- Wafers are sliced from the ingot
- Typically 300-600µm thick
Wafer Processing
Wafer Processing
Wafer Processing

- Why the trend to larger wafers?
  - More chips per wafer
  - Less waste

- After slicing
  - Lapping
  - Polishing
  - Defect detection
Semiconductor Processing

- Oxide Layer - SiO$_2$ (sand)
  - Heat Wafer in an oxidizing atmosphere - water vapor or pure oxygen gas

![Diagram of Oxide Layer on P-Type Silicon Wafer]
Semiconductor Processing

- How do you control where the features get placed?
  - Photolithography masks
Semiconductor Processing

- Need to remove the oxide layer
Semiconductor Processing

• Need to remove the oxide layer
Semiconductor Processing

- Need to remove the oxide layer
Semiconductor Processing

- Add polysilicon layer for gate
Semiconductor Processing

• Impurity injection
  – Diffusion
    • Wafers are placed in a heated tube with dopant gas
    • At high temperatures (~1000°C), the dopant diffuses into the exposed regions of the wafer
  – Ion Implantation
    • Dopants are introduced as ions into material by sweeping a beam across the material
    • Depth of implantation and density is controlled by the acceleration and exposure time
    • High energy implantation can cause lattice damage
  – Deposition
    • Deposit a gas or vapor (CVD) on the wafer at high temperatures
Semiconductor Processing

- Impurity injection
Semiconductor Processing

- Add Oxide insulation layer
Semiconductor Processing

- Add Metal layer
Semiconductor Processing

• pMOS Transistor
Interconnect

- Polysilicon to Metal contacts
- Diffusion to Metal contacts
- Diffusion to Polysilicon silicide contacts
- Metal to Metal vias
Metallization
Packaging Requirements

- **Electrical**: Low parasitics
- **Mechanical**: Reliable and robust
- **Thermal**: Efficient heat removal
- **Economical**: Cheap
Bonding Techniques

Wire Bonding

- Substrate
- Die
- Pad
- Lead Frame
Tape-Automated Bonding (TAB)

(a) Polymer Tape with imprinted wiring pattern.

(b) Die attachment using solder bumps.
Flip-Chip Bonding

Die

Solder bumps

Interconnect layers

Substrate
Package-to-Board Interconnect

(a) Through-Hole Mounting

(b) Surface Mount
Package Types
## Package Parameters

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Capacitance (pF)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>68 Pin Plastic DIP</td>
<td>4</td>
<td>35</td>
</tr>
<tr>
<td>68 Pin Ceramic DIP</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>256 Pin Pin Grid Array</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>Wire Bond</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Solder Bump</td>
<td>0.5</td>
<td>0.1</td>
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</tbody>
</table>

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])
Trends in Process Technology

- Copper Conductors
- Silicon on Insulator
- Strained Silicon
- Three-dimensional ICs
Multi-Chip Modules
## CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Well_Yellow.png" alt="Yellow" /></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Active_Area_Green.png" alt="Green" /></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Select_Green.png" alt="Green" /></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Polysilicon_Red.png" alt="Red" /></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Metal1_Blue.png" alt="Blue" /></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Metal2_Magenta.png" alt="Magenta" /></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Contact_To_Poly_Black.png" alt="Black" /></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Contact_To_Diffusion_Black.png" alt="Black" /></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td><img src="images/CMOS/CMOS_Process_Layers/Via_Black.png" alt="Black" /></td>
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</tbody>
</table>
Layers in 0.25 μm CMOS process

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>m1 m2 m3 m4 m5</td>
</tr>
<tr>
<td>well</td>
<td>nw</td>
</tr>
<tr>
<td>polysilicon</td>
<td>poly</td>
</tr>
<tr>
<td>contacts &amp; vias</td>
<td>ct</td>
</tr>
<tr>
<td></td>
<td>v12,v23,v34,v45</td>
</tr>
<tr>
<td>active area and FETs</td>
<td>ndif pdif nfct pfct</td>
</tr>
<tr>
<td>select</td>
<td>nplus pplus prb</td>
</tr>
</tbody>
</table>
Semiconductor Masks
Semiconductor Masks
Semiconductor Masks

n+ polycrystalline silicon contact
Semiconductor Masks

- n+
- metal
- polysilicon
- contact
Semiconductor Masks

- p+
- polysilicon
- metal
- contact
Semiconductor Masks

VIN - VDD

VOUT - VSS

VOUT - VSS
Design rules

• Design rules are critical to proper operation of the circuit

• They place restrictions on the sizes of layers and the distance between layers

• Often expressed in terms of $\lambda$ - half the minimum feature size
Design Rules

<table>
<thead>
<tr>
<th>MOSIS SCMOS Design Rules</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1  Contact size</td>
</tr>
<tr>
<td>5.2  Minimum poly overlap</td>
</tr>
<tr>
<td>5.3  Minimum contact spacing</td>
</tr>
<tr>
<td>5.4  Minimum spacing to gate of transistor</td>
</tr>
</tbody>
</table>

![Diagram showing design rules with dimensions 5.1, 5.2, 5.3, 5.4, and 5.5.](attachment:image.png)
CMOS Latchup

NMOS

P

S

G

D

n⁺

p⁺

Poly-Si

SIO₂

PMOS

B

S

G

D

S

G

D

B

n⁺

n

p⁺

p⁺

n⁺
CMOSLatchup
CMOS Latchup

- Acts like a SCR (silicon controlled rectifier)
- As long as both transistors are off, everything is fine
CMOS Latchup

- External disturbance causes current flow in $R_{\text{sub}}$ or $R_{\text{well}}$
- Feedback loop will cause the current draw to increase dramatically
CMOS Latchup

• External disturbances
  – ESD (electrostatic discharge) stress
  – Cosmic rays/alpha particles
  – Sudden transients on Vdd or Gnd
  – I/O pads interfacing with large currents off chip
CMOS Latchup

- Avoiding latchup
  - Decrease $R_{\text{sub}}$ and $R_{\text{well}}$ so that it is harder to turn on the BJT transistors
    - Place substrate and well contacts close together
    - Keep pMOS transistors close to Vdd and nMOS transistors close to ground
    - Surround transistors in I/O pads with guard rings
  - Decrease $\beta$ of BJT transistors
    - Space the pMOS and nMOS transistors apart
Next Class

• Performance Characterization

• Read Chapter 4