VLSI Design and Simulation

Lecture 2

MOS Transistor Theory
Lab

• Make sure that you have an engineering UNIX account

• Contact ECS if you don’t
MOS Transistor Theory

• Two types of transistors
  – nMOS
  – pMOS

• Digital integrated circuits use these transistors essentially as a voltage controlled switch
nMOS Transistor

• If the gate is “high”, the switch is on
• If the gate is “low”, the switch is off
nMOS Transistor

Body/Substrate (p)
nMOS Transistor

Body/Substrate (p)
nMOS Transistor
nMOS Transistor

[Diagram of an nMOS transistor with labels for Gate, Source, Drain, Oxide, Body/Substrate (p), n+, and Polycrystalline Silicon.]
nMOS Transistor

Accumulation Mode
nMOS Transistor

Accumulation Mode
nMOS Transistor

Depletion Mode

Gate

Source

Drain

Oxide

Depletion Region

$V_{GS} < V_T$
nMOS Transistor

Inversion Mode

Depletion Region

Inversion Region

Gate

Source

Drain

$V_{GS} > V_T$
nMOS Transistor

- Source
- Gate
- Oxide
- Drain
- Depletion Region
- Inversion Mode
- V_{GS} > V_T

nMOS Transistor
nMOS Transistor

Enhancement-mode

Depletion-mode
Threshold Voltage

• Dependent on
  – Gate conductor material
  – Gate insulator material
  – Channel Doping
  – Voltage difference between source and body
Threshold Voltage

\[ V_T = V_{T0} + \gamma \left( \sqrt{-2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) \]

• Threshold voltage is usually arrived at empirically
• \( \gamma \) is the body-effect coefficient and controls the impact of the source to bulk voltage
• \( \phi_F \) is the Fermi potential and is dependent on doping levels

\[ \phi_F = \frac{kT}{q} \ln \left( \frac{N_A}{N_i} \right) \]
pMOS Transistor

Accumulation Mode
pMOS Transistor

Enhancement-mode

Depletion-mode
nMOS Transistor

Linear or Nonsaturated Mode

nMOS Transistor

Gate

Source

Oxide

Drain

Depletion Region

$V_{GS} > V_T$

$V_{DS}$ small ($V_{GS} - V_{DS} > V_T$)

n+ n+ n+ n+
nMOS Transistor

Linear or Nonsaturated Mode

\[ V_{GS} > V_T \]

\[ V_{DS} = V_{GS} - V_T \]
nMOS Transistor

Saturated Mode

$V_{GS} > V_T$

$V_{DS}$ large ($V_{DS} > V_{GS} - V_T$)
MOS Transistor Parameters

Channel Length = L

Channel Width = W

Source

Drain
MOS Transistor Characteristics

- **Linear Mode**
- Assume both $V_{GS} > V_T$ and $V_{GD} > V_T$
- Assume that $V_T$ is constant for $x$ in $[0:L]$
- $V(0) = 0$ and $V(L) = V_{DS}$
MOS Transistor Characteristics

• Mobile electron charge

\[ Q_i(x) = -C_{ox} [V_G - V(x) - V_T] \]
MOS Transistor Characteristics

- Current is product of carrier drift velocity and available charge

\[ I_{DS} = -\nu(x)Q_i(x)W \]

\[ I_{DS} = -\mu_n \frac{dV}{dx} Q_i(x)W \]

\[ I_{DS} dx = -W\mu_n Q_i(x) dV \]

- Integrating along channel

\[ \int_0^L I_{DS} dx = -W\mu_n \int_0^{V_{DS}} Q_i(x) dV \]
MOS Transistor Characteristics

\[ \int_{0}^{L} I_{DS} dx = -W \mu_n \int_{0}^{V_{DS}} Q_i(x) dV \]

\[ I_{DS} L = W \mu_n \int_{0}^{V_{DS}} C_{ox} [V_{GS} - V(x) - V_T] dV \]

\[ I_{DS} L = W \mu_n C_{ox} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

\[ I_{DS} = k_n \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

\( k_n \) is the gain factor and is dependent on the transconductance \((\mu_n C_{ox})\) and the ratio between \(W\) and \(L\).
Example

• $\mu_n = 600 \text{ cm}^2/\text{V s}$
• $C_{\text{ox}} = 7 \times 10^{-8} \text{ F/cm}^2$
• $W = 20 \mu\text{m}$
• $L = 2 \mu\text{m}$

• $k_n = \mu_n C_{\text{ox}} \frac{W}{L} = 0.42 \text{ mA/V}^2$
MOS Transistor

![Graph of MOS Transistor Characteristics](image)
MOS Transistor
MOS Transistor

Linear

Saturated
MOS Transistor

- **Cutoff region** \((V_{GS} < V_T)\)
  \[ I_{DS} = 0 \]

- **Linear region** \((V_{GS} > V_T, V_{DS} < V_{GS} - V_T)\)
  \[ I_{DS} = k_n \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \]

- **Saturated region** \((V_{GS} > V_T, V_{DS} > V_{GS} - V_T)\)
  \[ I_{DS} = k_n \frac{(V_{GS} - V_T)^2}{2} \]
MOS Transistor

- Cutoff region \((V_{GS} < V_T)\)

  \[ S \quad \quad \quad D \]

- Linear region \((V_{GS} > V_T, V_{DS} < V_{GS} - V_T)\)

  \[ S \quad \quad \quad D \]

- Saturated region \((V_{GS} > V_T, V_{DS} > V_{GS} - V_T)\)

  \[ S \quad \quad \quad D \]
MOS Transistor Secondary Effects

- Body effect
- Channel-length modulation
- Drain punchthrough
- Impact ionization
- Velocity Saturation
Body effect

• We assumed that $V_{SB} = 0$ - i.e. the source potential equals the substrate potential

• In certain situations, this assumption is not true

• Has the effect of raising the threshold voltage
Channel-Length Modulation

- We previously assumed a constant $L$
- In reality, when $V_{DS} > (V_{GS} - V_T)$, the channel is pinched off and the effective channel length is reduced.
- Pinch off length is proportional to the square root of $V_{GS} - V_T$
- Net effect is that $I_{DS}$ is not constant in the saturated region.
MOS Transistor

- **Cutoff region** \((V_{GS}<V_T)\)

  \[ I_{DS} = 0 \]

- **Linear region** \((V_{GS}>V_T, \ V_{DS}<V_{GS}-V_T)\)

  \[ I_{DS} = k_n \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \]

- **Saturated region** \((V_{GS}>V_T, \ V_{DS}>V_{GS}-V_T)\)

  \[ I_{DS} = k_n \frac{(V_{GS} - V_T)^2}{2} \left( 1 + \lambda V_{DS} \right) \]
Channel-Length Modulation

![Graph showing channel-length modulation](image)
MOS Transistor

- Cutoff region \((V_{GS} < V_T)\)

- Linear region \((V_{GS} > V_T, V_{DS} < V_{GS} - V_T)\)

- Saturated region \((V_{GS} > V_T, V_{DS} > V_{GS} - V_T)\)
Drain punch-through

- For very large $V_{DS}$, the depletion region grows from the drain to the source
- Current flow increases rapidly
- $V_{GS}$ has no control on the current
- Potentially damaging to transistor
- Short channel effect
Impact ionization

- At small gate lengths, electric field becomes more pronounced
- Electrons get excited with enough energy to cause a substrate current
- This causes change of transistor parameters - threshold voltage, current flow, etc.
Velocity Saturation

• Assumption was that carrier velocity is proportional to electric field

• When channel is small, and the voltage is large, the velocity can saturate

\[ v = \begin{cases} 
\mu_n \xi & \xi < \xi_c \\
\mu_n \xi_c & \xi > \xi_c 
\end{cases} \]

\( \xi_c \) is value of electric field at which velocity saturates
MOS Transistor

- **Cutoff region** \((V_{GS} < V_T)\)
  \[ I_{DS} = 0 \]

- **Linear region** \((V_{GS} > V_T, \ V_{DS} < V_{GS} - V_T)\)
  \[ I_{DS} = k_n \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \]

- **Saturated region** \((V_{GS} > V_T, \ V_{DS} > V_{GS} - V_T)\)
  \[ I_{DS} = k_n \left[ (V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2} \right] \]
Velocity Saturation

\[ V_{GS} = V_{DD} \]

Long-channel device

Short-channel device

\[ V_{DSAT} \quad V_{GS} - V_T \quad V_{DS} \]
Velocity Saturation

\[ V_{DS} = V_{DSAT} \]

Linear

Velocity Saturated

\[ V_{DSAT} = V_{GT} \]

Saturated

\[ V_{DS} = V_{GT} \]
MOS Gain Characteristics

- **Transconductance** \( g_m = \frac{dI_{DS}}{dV_{GS}} \)
- **Cutoff region**
  \[ g_m = 0 \]
- **Linear region**
  \[ g_m = k_n V_{DS} \]
- **Saturated region**
  \[ g_m = k_n (V_{GS} - V_T) \]
CMOS Characteristics
nMOS Transistor

- **Cutoff region** \((V_{GSn} > V_{Tn})\)
  \[ I_{DSn} = 0 \]

- **Linear region** \((V_{GSn} < V_{Tn}, V_{DSn} > V_{GSn} - V_{Tn})\)
  \[ I_{DSn} = -k_n \left[ (V_{GSn} - V_{Tn}) V_{DSn} - \frac{V_{DSn}^2}{2} \right] \]

- **Saturated region** \((V_{GSn} < V_{Tn}, V_{DSn} < V_{GSn} - V_{Tn})\)
  \[ I_{DSn} = -k_n \frac{(V_{GSn} - V_{Tn})^2}{2} (1 + \lambda V_{DSn}) \]
pMOS Transistor

- **Cutoff region** \((V_{GSp} > V_{Tp})\)
  \[
  I_{DSp} = 0
  \]

- **Linear region** \((V_{GSp} < V_{Tp}, V_{DSp} > V_{GSp} - V_{Tp})\)
  \[
  I_{DSp} = k_p \left[ (V_{GSp} - V_{Tp})V_{DSp} - \frac{V_{DSp}^2}{2} \right]
  \]

- **Saturated region** \((V_{GSp} < V_{Tp}, V_{DSp} < V_{GSp} - V_{Tp})\)
  \[
  I_{DSp} = k_p \frac{(V_{GSp} - V_{Tp})^2}{2} \left(1 + \lambda V_{DSp} \right)
  \]
CMOS Inverter
CMOS Inverter
CMOS Inverter

\[ V_{GSn} = V_{in} \]
\[ V_{DSn} = V_{out} \]
\[ V_{GSp} = V_{in} - V_{DD} \]
\[ V_{DSP} = V_{out} - V_{DD} \]
\[ V_{tn} \approx V_{tp} \]
pMOS Transistor

- **Cutoff region** \((V_{in} > V_{DD} - V_T)\)
  \[ I_{DSP} = 0 \]

- **Linear region** \((V_{in} < V_{DD} - V_T, V_{out} > V_{in} + V_T)\)
  \[ I_{DS} = k_p \left[ (V_{in} - V_{DD} + V_T)(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2} \right] \]

- **Saturated region** \((V_{in} < V_{DD} - V_T, V_{out} < V_{in} + V_T)\)
  \[ I_{DS} = k_p \frac{(V_{in} - V_{DD} + V_T)^2}{2} \left( 1 + \lambda(V_{out} - V_{DD}) \right) \]
CMOS Inverter

![Graph showing CMOS inverter characteristics with various input voltages.](image)
CMOS Inverter
Next Class

• Noise Margin
• Static Load Inverters
• Read Chapter 5