1. Consider the following latch based pipeline. Assume that the input, \( IN \), is valid (i.e., set up) 2ns before the falling edge of \( CLK \) and is held till the falling edge of \( CLK \) (there is no guarantee on the value of \( IN \) at other times). Determine the maximum positive and negative skew on \( CLK' \) for correct functionality. The contamination delay is the minimum propagation delay through the combinational logic.

![Diagram of latch based pipeline]

2. For the circuit below, assume a unit delay through the register and logic blocks (i.e., \( t_{clk-q} = t_{logic} = 1 \)). Assume that the registers, which are positive edge-triggered, have a set-up time \( t_{su} \) of 1 and a hold time of 0. The delay through the multiplexer \( t_M \) equals 2.

![Diagram of circuit below]
a. Determine the minimum clock period. Disregard clock skew.
b. Repeat part a, factoring in a nonzero clock skew: \( \delta = t'_{\theta} - t_{\theta} = 1 \).
c. Repeat part a, factoring in a non-zero clock skew: \( \delta = t'_{\theta} - t_{\theta} = 4 \).
d. Derive the maximum positive clock skew that can be tolerated before the circuit fails.
e. Derive the maximum negative clock skew that can be tolerated before the circuit fails.

3. What are the advantages and disadvantages of ASIC standard cell design compared to full custom design?