Homework 5
Due March 29th

1. Design a finite state machine that controls the stop lights at a four-way intersection. One of the two streets is a main street that will always have green unless a car is present at the cross-street. Assume that the lights have only red and green. You should have two outputs (a R/G signal for each street) and two inputs (sensor inputs on each direction of the low-priority cross street.
   a. Show the Moore Machine FSM diagram
   b. Show the logic functions to realize the outputs and next state
   c. Show a PLA realization of the logic function. The PLA should be a NOR-NOR style implementation and should show all required transistors.
   d. In class a NOR-NOR implementation of a PLA was shown. It is possible to design a NAND-NAND implementation. Show what the structure of a NAND-NAND implementation would like for the logic functions you came up with in part b.

2. Consider the following layout for a 4x7 ROM array.

The red lines represent polysilicon word lines. The blue lines represent metal bit lines. At each intersection, underneath the metal is a transistor if necessary to wire a memory bit. The width of the transistor is .9µ and the length is .6µ. The distance between columns is 1.8µ and the distance between word lines is 2.1µ. Assume the resistance of polysilicon is 5Ω/square and the capacitance is .088 fF/µm², and the resistance and capacitance of metal are .1Ω/square and .041 fF/µm² respectively. Each transistor has a drain capacitance of .8 fF fF and an input gate capacitance of 0.4ff.
   a) What is the expected worst-case delay from the time a word-line is activated till the time that the data appears on the last bit line?
   b) What can you do to reduce the delay?
3. In class, the ROM array was shown with a pMOS transistor at the top of each row, and its gate was hardwired to ground. Are there any power dissipation issues with this configuration? Explain. Can you come up with a method to fix this problem.