Homework 4
Due March 17th

1. Compute the switching power consumed by the multiplexer shown above assuming that all significant capacitances have been lumped into the three shown capacitors where $C=0.3\text{pF}$. Assume that $V_{DD}=2.5\text{V}$ and the inputs $A, S, \text{ and } B$ are independent and uniformly distributed with events occurring at a frequency of 100MHz.

2. Design a 32-bit adder using a hierarchy of 4-bit carry lookahead adders. You do not need to show the transistor level detail, but show a block diagram showing the carry lookahead adders and the logic needed to connect them.

3. Design a pass-transistor network that implements the following function:
   
   $$S = ABC + \overline{A}BC + \overline{AB}C + \overline{ABC}$$

4. In the following circuit, assume that the inverter switches ideally at $V_{DD}/2$, and neglect channel modulation, and parasitic capacitance. The PMOS transistor is sized with a $W/L$ ratio of $1.5\mu\text{m}/0.25\mu\text{m}$, and the three NMOS transistors have a $W/L$ ratio of $0.5\mu\text{m}/0.25\mu\text{m}$, $V_{DD}=2.5\text{V}$, $V_{in}=0.5\text{V}$ and $V_{tp}=-0.4\text{V}$. 
a. What is the logic function performed by the circuit
b. Explain why and under what conditions the circuit has non-zero static dissipation
c. Using 1 transistor, design a fix so that there will be no static dissipation. Make sure to explain any transistor sizing that may be necessary.

5. a. Implement the two logic functions $F = A + B + C$ and $G = F + D$ in two stages of cascaded domino logic to minimize transistor count. Show all the required MOS transistors. The design must have at least two stages.
   b. Design a np-CMOS or zipper version of the same logic