

**Errata to**

*MPCFPE32BAD/AD*  
*Rev. 0, 10/2002*

*Errata to*  
*Programming Environments*  
*Manual for 32-Bit*  
*Implementations of the*  
*PowerPC Architecture, Rev. 2*



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This errata describes corrections to the *Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture, Rev 2*. For convenience, the section number and page number of the errata item in the programming manual are provided.

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Section, Page No.	Changes
4.4.3.1,4-63	<p>In Table 4-37, add the following two sentences to the end of the <b>dcbi</b> operation:</p> <p>Note that some implementations may execute this instruction as a <b>dcbf</b>. This instruction is optional.</p>
7.1,7-1	<p>Replace the fourth paragraph with the following:</p> <p>The segment information, used to generate the interim virtual addresses, is stored as segment descriptors. These descriptors may reside in on-chip segment registers (32-bit implementations).</p>
7.3.1.1, 7-3	Remove this section.
8.2, 8-24	<p>Replace the target address <b>CTR</b>    0b00 of <b>bcctr</b> with <b>CTR[0–29]</b>    0b00, the code sequence should read as follows:</p> <pre data-bbox="565 701 1114 831"> cond_ok ← BO[0]   (CR[BI] ≡ BO[1]) if cond_ok then NIA ←iea CTR[0-29]    0b00 if LK then LR ←iea CIA + 4 </pre>
8.2, 8-26	<p>In the first sentence after Table 8-9, replace the target address <b>CTR</b>    0b00 of <b>bcctr</b> with <b>CTR[0–29]</b>    0b00. The sentence should read as follows:</p> <p>The branch target address is <b>CTR[0–29]</b>    0b00.</p>
8.2, 8-26	<p>Replace the target address <b>LR</b>    0b00 of <b>bclr</b> with <b>CTR[0–29]</b>    0b00, the code sequence should read as follows:</p> <pre data-bbox="565 1138 1149 1327"> if ¬ BO[2] then CTR ← CTR - 1 ctr_ok ← BO[2]   ((CTR ≠ 0) ⊕ BO[3]) cond_ok ← BO[0]   (CR[BI] ≡ BO[1]) if ctr_ok &amp; cond_ok then NIA ←iea LR[0-29]    0b00 if LK then LR ←iea CIA + 4 </pre>
8.2, 8-25	<p>In the first sentence after Table 8-11, replace the target address <b>LR</b>    0b00 of <b>bclr</b> with <b>LR[0–29]</b>    0b00. The sentence should read as follows:</p> <p>The branch target address is <b>LR[0–29]</b>    0b00.</p>
8.2, 8-43	<p>Add the following two sentences to the end of the <b>dcbi</b> description:</p> <p>Note that some implementations may execute this instruction as a <b>dcbf</b>. This instruction is optional.</p>

Section, Page No.	Changes
8.2, 8-44	<p data-bbox="495 157 1258 199">After the third paragraph, add the following paragraph:</p> <p data-bbox="495 210 1438 378">The coherency state of a cache block after a write access (caused by a <b>dcbst</b>) is implementation-dependent. For example, some implementations may mark the cache block exclusive, where others may mark it invalid.</p>
8.2, 8-163	<p data-bbox="495 388 1438 472">Replace the first sentence of the only paragraph, the sentence should read as follows:</p> <p data-bbox="495 483 1438 567">The contents of <b>rS</b> are shifted right the number of bits specified by <b>rB[27–31]</b>.</p>

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