ECE 3401 Spring 2009
Digital Systems Design
T/Th 11 AM-12:15 PM ITE 125

Instructor: Prof. Yunsi Fei
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Instructor’s office hours: T/Th 5-6pm, or upon appointments, @ ITEB 439.

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TA’s office hours: TBD.

Lab: ITE C30

Course Description: Design and evaluation of control and data structures for digital systems. Hardware design languages are used to describe and design both behavioral and register transfer level architectures and control units with a microprogramming emphasis. Cover basic computer architecture, memories, digital interfacing, timing and synchronization, and microprocessor systems. (three credits)

All the course materials (slides, assignments, discussions, etc.) will be provided on HuskyCT. (http://huskyct.uconn.edu)

Prerequisites: CSE 2300 W (old number: 210W) - Digital Logic Design


Reference The Student's Guide to VHDL by Peter J. Ashenden, Morgan Kaufmann.

Software Tools: The course is very tool-intensive. Homework will include designing and simulating some functional modules by using hardware description languages. We will use Xilinx ISE and ModelSim simulator. http://www.xilinx.com/ise/webpack

Grading: Homework (about 9) and pop quizzes 20%
Midterm exam (~ Mar. 5th, 2009) 25%
Final project design 25%
Final Exam (~ May 6th, 2009) 30%
**Rules:** Participation in class discussion is strongly encouraged. Homework is due at the beginning of class on the due date, no extensions. Turn cell phones and MP3s (iPods) off during class.

**Topics:**
- Overview of digital systems
- Combinational logic circuits and design
- FPGA & CPLD
- VHDL Description Of Digital Systems - Behavioral Modeling
- VHDL Description Of Digital Systems - Structural Modeling
- VHDL Description OF Arithmetic Functions
- Sequential circuits
- Sequential system design, processor datapath and control unit
- Memory and timing issues
- Computer design basic
- Instruction set architecture
- Pipeline design
- Verilog basics (optional)
- I/O, bus design, D/A, A/D, power issues (optional)