

ECE 252 Spring 2007
Digital Systems Design
T/Th 11 AM-12:15 PM CAST204

Instructor: Prof. Yunsi Fei
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TA's office hours : T/W 1-2pm @ BECAT A65

Lab: ITE C30

Course Description: Design and evaluation of control and data structures for digital systems. Hardware design languages are used to describe and design both behavioral and register transfer level architectures and control units with a microprogramming emphasis. Cover basic computer architecture, memories, digital interfacing, timing and synchronization, and microprocessor systems. (*three credits*)

All the course materials (slides, assignments, discussions, etc.) will be provided on WebCT. (<http://vista.uconn.edu>)

Prerequisites: CSE 210W (Digital Logic Design)

Text:

1. *Logic and Computer Design Fundamentals* by M. Morris Mano and Charles R. Kime, 3rd Edition, Pearson Prentice Hall.
 - Companion website: <http://www.writphotec.com/mano/>
2. *The Student's Guide to VHDL* by Peter J. Ashenden, Morgan Kaufmann.

Software Tools: The course is very tool-intensive. Homework will include designing and simulating some functional modules by using hardware description language. We will use Xilinx ISE and ModelSim simulator. <http://www.xilinx.com/ise/webpack>

<u>Grading:</u>	Homework (about 9) and quizzes	20%
	Midterm exam (Mar. 1 st)	25%
	Final project design	25%

Final Exam (around May 3rd, 2007)

30%

Rules:

Participation in class discussion is strongly encouraged. Homework is due at the beginning of class on the due date, no extensions. Turn cell phones off during class.

Topics:

Overview of computer systems and information representations
Combinational logic circuits and design
FPGA & CPLD
VHDL Description Of Digital Systems - Behavioral Modeling
VHDL Description Of Digital Systems - Structural Modeling
VHDL Description OF Arithmetic Functions
Sequential circuits
Sequential system design, processor datapath and control unit
Memory and timing issues
Computer design basic
Instruction set architecture
Pipeline design
Verilog basics
I/O, bus design, D/A, A/D, power issues (optional)