

ECE 252 Spring 2006
Digital Systems Design
Th 6-8:30 pm ITE 127

Instructor: Prof. Yunsi Fei
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Office Hours: TBD

Course Description: Design and evaluation of control and data structures for digital systems. Hardware design languages are used to describe and design both behavioral and register transfer level architectures and control units with a microprogramming emphasis. Cover basic computer architecture, memories, digital interfacing, timing and synchronization, and microprocessor systems. (*three credits*)

All the course materials (slides, assignments, discussions, etc.) will be provided on WebCT. (<http://vista.uconn.edu>)

Prerequisites: CSE 210W (Digital Logic Design)

Text:

1. *Logic and Computer Design Fundamentals* by M. Morris Mano and Charles R. Kime, 3rd Edition, Pearson Prentice Hall.
 - Companion website: <http://www.writphotec.com/mano/>
2. *The Designer's Guide to VHDL* by Peter J. Ashenden, 2nd Edition, Morgan Kaufmann.

Software Tools: The course is very tool-intensive. Homework will include designing and simulating some functional modules by using hardware description language. We will use Xilinx ISE and ModelSim simulator. <http://www.xilinx.com/ise/webpack>

Grading:

Homework (about 9) and quizzes	20%
Midterm exam (Mar. 2nd)	25%
Final project design	25%
Final Exam (around May 4 th , 2006)	30%

The normal plus/minus system will be applied:

70-72=C-, 73-76=C, 77-79=C+
80-82=B-, 83-86=B, 87-89=B+
90-92=A-, 93-96=A, 97-100=A+

Rules: Participation in class discussion is strongly encouraged. Homework is due at the beginning of class on the due date, no extensions. Turn cell phones off during class.

Topics:
 Overview of computer systems and information representations
 Combinational logic circuits and design
 FPGA & CPLD
 VHDL Description Of Digital Systems - Behavioral Modeling
 VHDL Description Of Digital Systems - Structural Modeling
 VHDL Description OF Arithmetic Functions
 Sequential circuits
 Sequential system design, processor datapath and control unit
 Memory and timing issues
 Computer design basic
 Instruction set architecture
 Pipeline design
 Verilog basics
 I/O, bus design, D/A, A/D, power issues (optional)

Tentative Schedule:

Week	Date	Content	
1	Jan 19	Overview	
2	Jan 26	Combinational circuits, FPGA	
3	Feb 2	VHDL basics	
4	Feb 9	VHDL	
5	Feb 16	VHDL	
6	Feb 23	Sequential circuits	
7	Mar 2		Midterm EXAM
8	Mar 9		Spring Break
9	Mar 16	Sequential system design	
10	Mar 23	Memory and timing	
11	Mar 30	Computer design basic	
12	Apr 6	Instruction set architecture	
13	Apr 13	Pipelined Design	
14	Apr 20	I/O, bus, D/A, etc.	
15	Apr 27	Verilog basics, wrap-up	
16	May 4 (6-8pm)		FINAL EXAM