ECE 6095: Special Topics in Computer Engineering: VLSI Design Verification and Testing

Instructor: Prof. Mohammad Tehranipoor

Date	Description	HW	Due (4pm)
Week 1 Sep. 1	First Class, Introduction Test Process and Equipment		
Week 2 Sep. 8	Test Economics Logic and Fault Modeling	**HW1**	**Due in one week**
Week 3 Sep. 15	Logic and Fault Modeling Fault Simulation		
Week 4 Sep. 22	Combinational ATPG Basics Combinational ATPG Basics	**HW2**	**Due in two weeks**
Week 5 Sep. 29	Combinational ATPG ATPG Systems and Testability Measures		
Week 6 Oct. 6	ATPG Systems and Testability Measures Sequential Circuit ATPG	**HW3**	**Due in one week**
Week 7 Oct. 13	Discuss Final Project Physical Design and ATPG Tool	**HW4 Final Project**	**Due in two weeks**
Week 8 Oct. 20	Functional Testing Design-for-testability (DFT) I		
Week 9 Nov. 3	DFT II Delay Test		
Week 10 Nov. 10	Delay Test I_{DDQ} Current Testing	**HW5 Final project quick update**	**Due in two weeks**
Week 11 Nov. 17	Memory Testing Memory Testing		
Break	Thanksgiving break		
Week 12 Dec. 1	**Exam** Project Presentations	**HW6**	**Due in two weeks**
Week 13 Dec. 8	Built-In Self-Test (BIST) I BIST II		
Discussion Class	Boundary Scan, Nanotechnology problems–Research Opportunities		
Dec. 20	**Project Demonstration**		

First class: Sep. 1, 2009 **Last class: Dec. 8, 2009**

 # Quizes: 2-3 **Office Hours: Tu 2-3pm**

 # HWs: 5-6