VLSI Design Verification and Testing

Delay Test

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Delay Test

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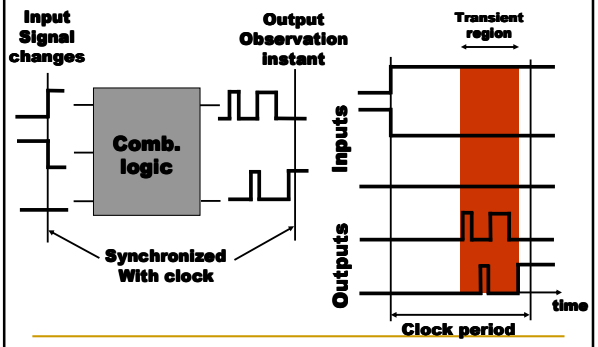
- Circuit delays and event propagation
- *Path-delay tests*
  - *Non-robust test*
  - *Robust test*
  - Five-valued logic and test generation
- *Path-delay fault* (PDF) and other fault models
- Test application methods
  - Combinational, enhanced-scan and normal-scan
  - Variable-clock and rated-clock methods
- At-speed test
- Timing design and delay test
- Summary

Delay Test Definition

- A circuit that passes delay test must produce correct outputs when inputs are applied and outputs observed with specified timing.
- For a combinational or synchronous sequential circuit, delay test verifies the limits of delay in combinational logic.
- Delay test problem for asynchronous circuits is complex and not well understood.

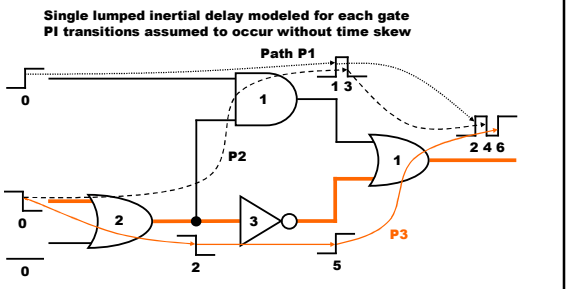
Digital Circuit Timing



Circuit Delays

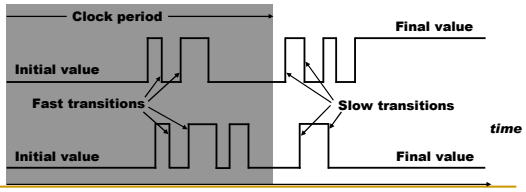
- Switching or inertial delay is the interval between input change and output change of a gate:
  - Depends on input capacitance, device (transistor) characteristics and output capacitance of gate.
  - Also depends on input rise or fall times and states of other inputs (second-order effects).
  - Approximation: fixed rise and fall delays (or min-max delay range, or single fixed delay) for gate output.
- Propagation or interconnect delay is the time a transition takes to travel between gates:
  - Depends on transmission line effects (distributed *R*, *L*, *C* parameters, length and loading) of routing paths.
  - Approximation: modeled as lumped delays for gate inputs.
- See Section 5.3.5 for timing models.

Event Propagation Delays



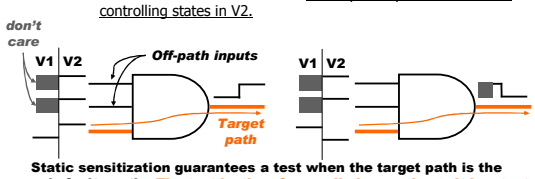
Circuit Outputs

- Each path can potentially produce one signal transition at the output.
- The location of an output transition in time is determined by the delay of the path.



Singly-Testable Paths (Non-Robust Test)

- The delay of a target path is tested if the test propagates a transition via path to a path destination.
- Delay test is a combinational vector-pair, V1,V2, that:
  - Produces a transition at path input.
  - Produces static sensitization -- All off-path inputs assume non-controlling states in V2.



Static sensitization guarantees a test when the target path is the only faulty path. The test is, therefore, called *non-robust*. It is a test with minimal restriction. A path with no such test is a *false path*.

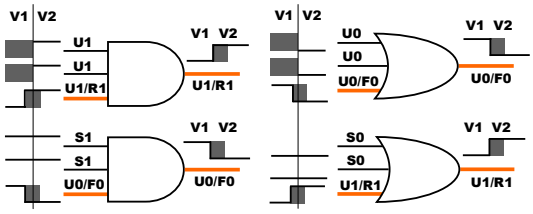
See Figure 12.4, page 422

Robust Test

- A robust test guarantees the detection of a delay fault of the target path, irrespective of delay faults on other paths.
- A robust test is a combinational vector-pair, V1, V2, that satisfies following conditions:
  - Produce *real events* (different steady-state values for V1 and V2) on all on-path signals.
  - All on-path signals must have *controlling events* arriving via the target path.
- A robust test is also a non-robust test.
- Concept of robust test is general – robust tests for other fault models can be defined.

Robust Test Conditions

- Real events on target path.
- Controlling events via target path.



A Five-Valued Algebra

- Signal States: S0, U0 (F0), S1, U1 (R1), XX.
- On-path signals: **F0** and **R1**.
- Off-path signals: **F0=U0** and **R1=U1**.

AND

Input 2 \ Input 1	S0	U0	S1	U1	XX
S0	S0	S0	S0	S0	S0
U0	S0	U0	U0	U0	U0
S1	S0	U0	S1	U1	XX
U1	S0	U0	U1	U1	XX
XX	S0	U0	XX	XX	XX

OR

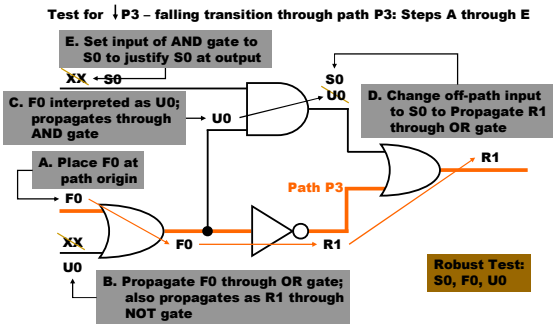
Input 2 \ Input 1	S0	U0	S1	U1	XX
S0	S0	U0	S1	U1	XX
U0	U0	U0	S1	U1	XX
S1	S1	S1	S1	S1	S1
U1	U1	U1	S1	U1	U1
XX	XX	XX	S1	U1	XX

NOT

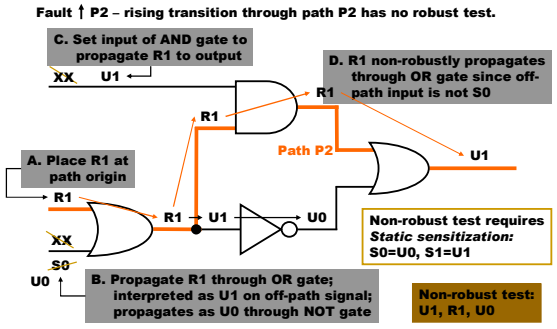
Input	S0	U0	S1	U1	XX
	S1	U1	S0	U0	XX

Ref.: Lin-Reddy *IEEETCAD*-87

Robust Test Generation



Non-Robust Test Generation



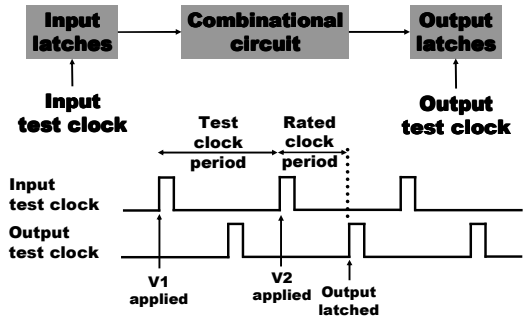
Path-Delay Faults (PDF)

- Two PDFs (rising and falling transitions) for each physical path.
- Total number of paths is an exponential function of gates. Critical paths, identified by static timing analysis (e.g., *Primetime* from Synopsys), must be tested.
- PDF tests are delay-independent. Robust tests are preferred, but some paths have only non-robust tests.
- Three types of PDFs (Gharaybeh, et al., *JETTA* (11), 1997):
  - *Singly-testable* PDF – has a non-robust or robust test.
  - *Multiply-testable* PDF – a set of singly untestable faults that has a non-robust or robust test. Also known as functionally testable PDF.
  - *Untestable* PDF – a PDF that is neither singly nor multiply testable.
- A singly-testable PDF has at least one *single-input change* (SIC) non-robust test.

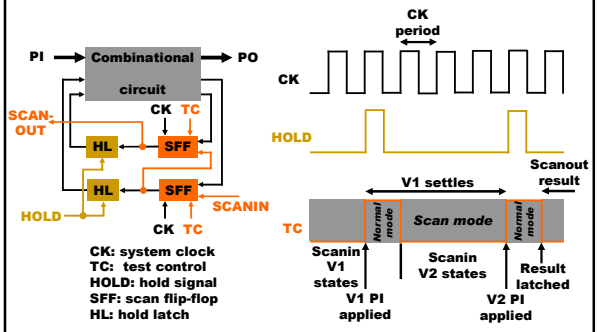
Other Delay Fault Models

- *Segment-delay* fault -- A segment of an I/O path is assumed to have large delay such that all paths containing the segment become faulty.
- *Transition* fault -- A segment-delay fault with segment of unit length (single gate):
  - Two faults per gate; slow-to-rise and slow-to-fall.
  - Tests are similar to stuck-at fault tests. For example, a line is initialized to 0 and then tested for s-a-0 fault to detect slow-to-rise transition fault.
  - Models spot (or gross) delay defects.
- *Line-delay* fault – A transition fault tested through the longest delay path. Two faults per line or gate. Tests are dependent on modeled delays of gates.
- *Gate-delay* fault – A gate is assumed to have a delay increase of certain amount (called *fault size*) while all other gates retain some nominal delays. Gate-delay faults only of certain sizes may be detectable.

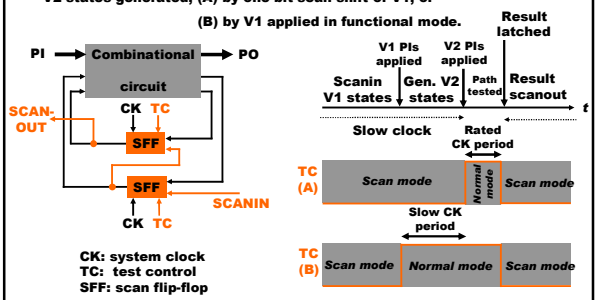
Slow-Clock Test



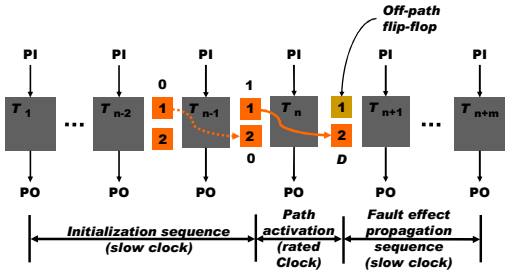
Enhanced-Scan Test



Normal-Scan Test



Variable-Clock Sequential Test



Note: Slow-clock makes the circuit fault-free in the presence of delay faults.

Variable-Clock Models

- Fault effect propagation can be affected by ambiguous states of off-path flip-flops at the end of the rated-clock time-frame (Chakraborty, *et al.*, *IEEETCAD*, Nov. 1997):
  - Fault model A – Off-path flip-flops assumed to be in correct states; *sequential non-robust test* (optimistic).
  - Fault model B – Off-path flip-flops assumed to be in unknown state; *sequential robust test* (pessimistic).
  - Fault model C – Off-path flip-flops in steady (hazard-free) state retain their correct values, while others assume unknown state; *sequential robust test*.
- Test length: A test sequence of N vectors is repeated N times, with a different vector applied at rated-clock each time.
  - Test time ~ N^2 x (slow-clock period)

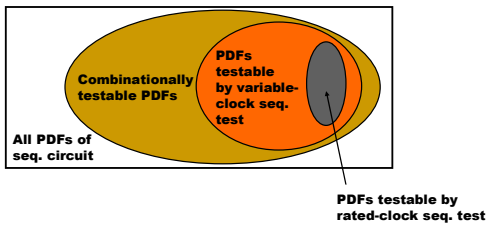
Variable-Clock Example

- ISCAS'89 benchmark s35932 (non-scan).
- 2,124 vectors obtained by simulator-selection from random vectors (Parodi, *et al.*, ITC-98).
- PDF coverage, 26,228/394,282 ~ 6.7%
- Longest tested PDF, 27 gates; longest path has 29 gates.
- Test time ~ 4,511,376 clocks.

Rated-Clock Sequential Test

- All vectors are applied with rated-clock.
- Paths are singly and multiply activated potentially in several time-frames.
- Test generation requires a 41-valued logic (Bose, *et al.*, *IEEETVLSI*, June 1998).
- Test generation is extremely complex for non-scan circuits (Bose and Agrawal, ATS-95).
- Fault simulators are effective but work with conservative assumptions (Bose, *et al.*, *IEEETVLSI*, Dec. 1993; Parodi, *et al.*, ITC-98).

Comparing PDF Test Modes



Ref.: Majumder, *et al.*, VLSI Design - 98

At-Speed Test

- At-speed test means application of test vectors at the rated-clock speed.
- Two methods of at-speed test.
- External test:
  - Vectors may test one or more functional critical (longest delay) paths and a large percentage (~100%) of transition faults.
  - High-speed testers are expensive.
- *Built-in self-test* (BIST):
  - Hardware-generated random vectors applied to combinational or sequential logic.
  - Only clock is externally supplied.
  - Non-functional paths that are longer than the functional critical path can be activated and cause a good circuit to fail.
  - Some circuits have initialization problem.

Timing Design & Delay Test

- Timing simulation:
  - Critical paths are identified by static (vector-less) timing analysis tools like *Primetime* (Synopsys).
  - Timing or circuit-level simulation using designer-generated functional vectors verifies the design.
- Layout optimization: Critical path data are used in placement and routing. Delay parameter extraction, timing simulation and layout are repeated for iterative improvement.
- Testing: Some form of at-speed test is necessary. PDFs for critical paths and all transition faults are tested.

Summary

- *Path-delay fault* (PDF) models distributed delay defects. It verifies the timing performance of a manufactured circuit.
- *Transition fault* models spot delay defects and is testable by modified stuck-at fault tests.
- Variable-clock method can test delay faults but the test time can be long.
- Critical paths of non-scan sequential circuits can be effectively tested by rated-clock tests.
- Delay test methods (including BIST) for non-scan sequential circuits using slow ATE require investigation:
  - Suppression of non-functional path activation in BIST.
  - Difficulty of rated-clock PDF test generation.
  - Long sequences of variable-clock tests.