VLSI Design Verification and Testing

Design for Testability (DFT) - 2

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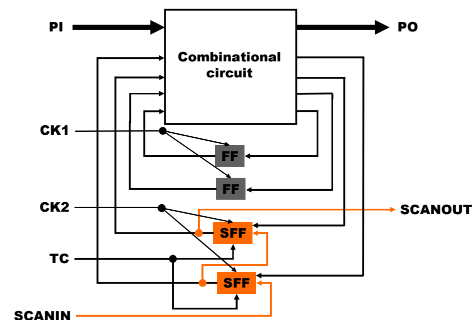
Overview: Partial-Scan & Scan Variations

- Definition
- *Partial-scan* architecture
- Scan flip-flop selection methods
- Cyclic and acyclic structures
- Partial-scan by cycle-breaking
- Scan variations
- *Scan-hold flip-flop* (SHFF)
- Summary

Partial-Scan Definition

- A subset of flip-flops is scanned.
- Objectives:
  - Minimize area overhead and scan sequence length, yet achieve required fault coverage
  - Exclude selected flip-flops from scan:
    - Improve performance
    - Allow limited scan design rule violations
  - Allow automation:
    - In scan flip-flop selection
    - In test generation
  - Shorter scan sequences – reduce application time

Partial-Scan Architecture



Scan Flip-Flop Selection Methods

- Testability measure based:
  - Use of SCOAP: limited success.
- Structure based:
  - Cycle breaking
  - Balanced structure
    - Sometimes requires high scan percentage
- ATPG based:
  - Use of combinational and sequential TG

Cycle Breaking

- Difficulties in ATPG
- S-graph and MFVS problem
- Test generation and test statistics
- Partial vs. full scan
- Partial-scan flip-flop

Difficulties in Seq. ATPG

- Poor initializability.
- Poor controllability/observability of state variables.
- Gate count, number of flip-flops, and sequential depth do not explain the problem.
- Cycles are mainly responsible for complexity.
- A Sequential ATPG experiment:

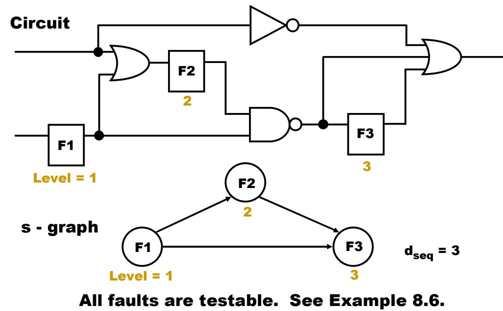
	Circuit	Number of gates	Number of flip-flops	Sequential depth	ATPG CPU s	Fault coverage
Cyclic	TLC	355	21	14*	1,247	89.01%
Acyclic	Chip A	1,112	39	14	269	98.80%

** Maximum number of flip-flops on a PI to PO path*

Benchmark Circuits

Circuit	s1196	s1238	s1488	s1494
PI	14	14	8	8
PO	14	14	19	19
FF	18	18	6	6
Gates	529	508	653	647
Structure	Cycle-free	Cycle-free	Cyclic	Cyclic
Sequential depth	4	4	--	--
Total faults	1242	1355	1486	1506
Detected faults	1239	1283	1384	1379
Potentially detected faults	0	0	2	2
Untestable faults	3	72	26	30
Abandoned faults	0	0	76	97
Fault coverage (%)	99.8	94.7	93.1	91.6
Fault efficiency (%)	100.0	100.0	94.8	93.4
Max. sequence length	3	3	24	28
Total test vectors	313	308	525	559
Gentest CPU s (Sparc 2)	10	15	19941	19183

Cycle-Free Example



All faults are testable. See Example 8.6.

Relevant Results

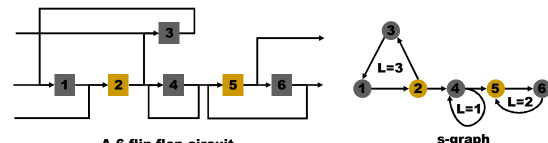
- **Theorem 8.1**: A cycle-free circuit is always initializable. It is also initializable in the presence of any non-flip-flop fault.
- **Theorem 8.2**: Any non-flip-flop fault in a cycle-free circuit can be detected by at most $d_{seq} + 1$ vectors.
- **ATPG complexity**: To determine that a fault is untestable in a cyclic circuit, an ATPG program using nine-valued logic may have to analyze 9^{Nff} time-frames, where Nff is the number of flip-flops in the circuit.

A Partial-Scan Method

- Select a minimal set of flip-flops for scan to eliminate all cycles.
- Alternatively, to keep the overhead low only long cycles may be eliminated.
- In some circuits with a large number of self-loops, all cycles other than self-loops may be eliminated.

The MFVS Problem

- For a directed graph find a set of vertices with smallest cardinality such that the deletion of this vertex-set makes the graph acyclic.
- The *minimum feedback vertex set* (MFVS) problem is NP-complete; practical solutions use heuristics.
- A secondary objective of minimizing the depth of acyclic graph is useful. This further reduces time to generate patterns.



A 6-flip-flop circuit **s-graph**

cardinality of a set is a measure of the "number of elements of the set".

Test Generation

- Scan and non-scan flip-flops are controlled from separate clock PIs:
  - Normal mode – Both clocks active
  - Scan mode – Only scan clock active
- Seq. ATPG model:
  - Scan flip-flops replaced by PI and PO
  - Seq. ATPG program used for test generation
  - Scan register test sequence, 001100…, of length $n_{sff} + 4$ applied in the scan mode
  - Each ATPG vector is preceded by a scan-in sequence to set scan flip-flop states
  - A scan-out sequence is added at the end of each vector sequence
- Test length = $(n_{ATPG} + 2)\, n_{sff} + n_{ATPG} + 4$ clocks

Same as full scan except that n_{sff} is significantly smaller

Partial Scan Example

- Circuit: TLC
- 355 gates
- 21 flip-flops

Scan flip-flops	Max. cycle length (L)	Depth*	ATPG CPU s	Fault sim. CPU s	Fault cov.	ATPG vectors	Test seq. length
0	4	14	1,247	61	89.01%	805	805
4	2	10	157	11	95.90%	247	1,249
9	1	5	32	4	99.20%	136	1,382
10	1	3	13	4	100.00%	112	1,256
21	0	0	2	2	100.00%	52	1,190

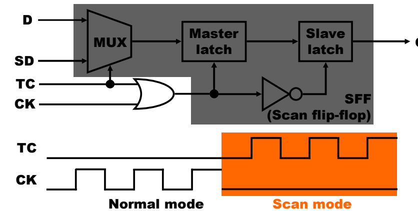
* Cyclic paths ignored

Partial vs. Full Scan: S5378

	Seq ATPG Original	Partial-scan	Full-scan
Number of combinational gates	2,781	2,781	2,781
Number of non-scan flip-flops (10 gates each)	179	149	0
Number of scan flip-flops (14 gates each)	0	30	179
Gate overhead	0.0%	2.63%	15.66%
Number of faults	4,603	4,603	4,603
PI/PO for ATPG	35/49	65/79	214/228
Fault coverage	70.0%	93.7%	99.1%
Fault efficiency	70.9%	99.5%	100.0%
CPU time on SUN Ultra II 200MHz processor	5,533 s	727 s	5 s
Number of ATPG vectors	414	1,117	585
Scan sequence length	414	34,691	105,662

Flip-flop for Partial Scan

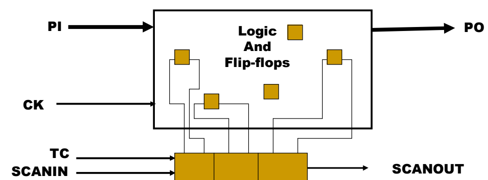
- Normal scan flip-flop (SFF) with multiplexer of the LSSD flip-flop is used.
- Scan flip-flops require a separate clock control:
  - Either use a separate clock pin
  - Or use an alternative design for a single clock pin



Scan Variations

- Integrated and Isolated scan methods
  - Scan path: NEC 1968
  - Serial scan: 1973
  - LSSD: IBM 1977
  - **Scan set**: Univac 1977
  - RAS: Fujitsu/Amdahl 1980

Scan Set



Scan Set Applications

- Advantages
  - Potentially useable in delay testing.
  - Concurrent testing: can sample the system state while the system is running
    - Used in *microrollback*
- Disadvantages
  - Higher overhead due to routing difficulties

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Random-Access Scan (RAS)

- The scan function is implemented like a random-access memory (RAM)
- All flip-flops form a RAM in scan mode
- A subset of flip-flops can be included in the RAM if partial scan is desired
- In scan mode, any flip-flop can be read or written

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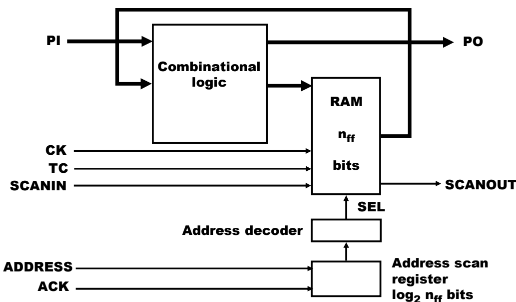
Random-Access Scan (RAS)



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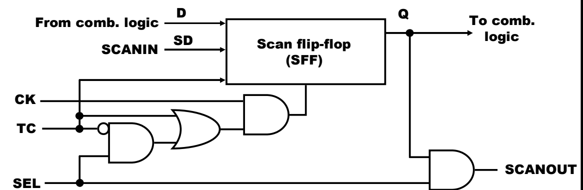
RAS Flip-Flop (RAM Cell)



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RAS Applications

- Logic test: reduced test length. We don’t have shift an entire pattern again as in full scan method. Only the differences between existing data in flip-flops
- Delay test: Easy to generate *single-input-change* (SIC) delay tests.
- Advantage:
  - RAS may be suitable for certain architecture, e.g., where memory is implemented as a RAM block.
- Disadvantages:
  - Not suitable for random logic architecture
  - High overhead – gates added to SFF, address decoder, address register, extra pins and routing

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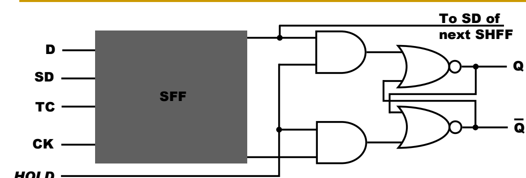
Scan-Hold Flip-Flop (SHFF)



- The control input *HOLD* keeps the output steady at previous state of flip-flop.
- Applications:
  - Reduce power dissipation during scan
  - Isolate asynchronous parts during scan test
  - Delay testing

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Summary

- Partial-scan is a generalized scan method; scan can vary from 0 to 100%.
- Elimination of long cycles can improve testability via sequential ATPG.
- Elimination of all cycles and self-loops allows combinational ATPG.
- Partial-scan has lower overheads (area and delay) and reduced test length.
- Partial-scan allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned.