VLSI Design Verification and Testing

Design for Testability (DFT) - 1

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Overview

- Definition
- Ad-hoc methods
- *Scan design*
  - Design rules
  - Scan register
  - Scan flip-flops
  - Scan test sequences
  - Overhead
  - Scan design system
- Summary

Definition

- *Design for testability* (DFT) refers to those design techniques that make test generation and test application cost-effective.
- DFT methods for digital circuits:
  - Ad-hoc methods
  - Structured methods:
    - *Scan*
    - *Partial Scan*
    - *Built-In Self-Test (BIST)*
    - *Boundary Scan*

Ad-Hoc DFT Methods

- Good design practices learned through experience are used as guidelines:
  - **Don't-s** and Do-s
    - Avoid asynchronous (unclocked) feedback.
    - Avoid delay dependant logic.
    - Avoid parallel drivers.
    - Avoid monostables and self-resetting logic.
    - Avoid gated clocks.
    - Avoid redundant gates.
    - Avoid high fanin fanout combinations.

Ad-Hoc DFT Methods

- Good design practices learnt through experience are used as guidelines:
  - Don't-s and **Do-s** (contd.)
    - Make flip-flops initializable.
    - Separate digital and analog circuits.
    - Provide test control for difficult-to-control signals.
    - Buses can be useful and make life easier.
    - Limit gate fanin and fanout.
    - Consider ATE requirements (tristates, etc.)

Ad-Hoc DFT Methods

- Design Reviews
  - Manual analysis
    - Conducted by experts
  - Programmed analysis
    - Using design auditing tools
  - Programmed enforcement
    - Must use certain design practices and cell types.
- Objective: Adherence to design guidelines and testability improvement techniques with little impact on performance and area.

Ad-Hoc DFT Methods

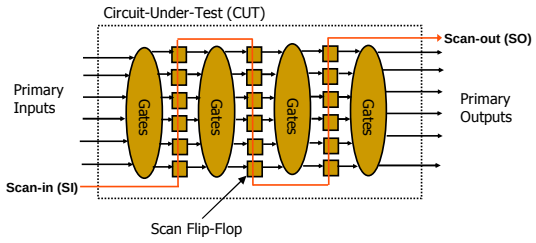
- Disadvantages of ad-hoc DFT methods:
  - Experts and tools not always available
  - Test generation is often manual with no guarantee of high fault coverage
    - Functional patterns
  - Design iterations may be necessary
  - Very time consuming

Scan Design

- Objectives
  - Simple read/write access to all or subset of storage elements in a design.
  - Direct control of storage elements to an arbitrary value (0 or 1).
  - Direct observation of the state of storage elements and hence the internal state of the circuit.

Key is – Enhanced controllability and observability.

Scan Design



Scan Design

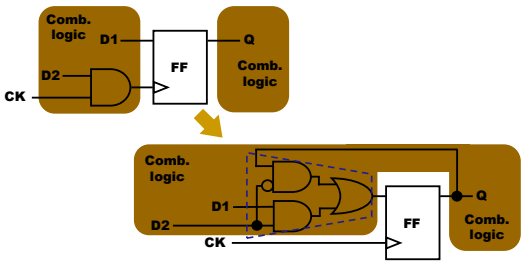
- Circuit is designed using pre-specified design rules.
- Test structure (hardware) is added to the verified design:
  - Add one (or more) *test control* (TC) primary input.
  - Replace flip-flops by *scan flip-flops* and connect to form one or more shift registers in the test mode.
  - Make input/output of each scan shift register controllable/observable from PI/PO.
- Use combinational ATPG to obtain tests for all testable faults in the combinational logic.
- Add shift register tests and convert ATPG tests into scan sequences for use in manufacturing test.

Scan Design Rules

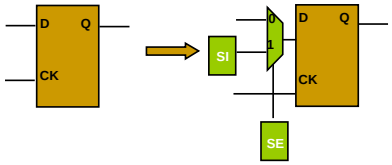
- Use only clocked D-type flip-flops for all state variables.
- At least one PI pin must be available for test; more pins, if available, can be used.
- All clocks must be controlled from PIs.
- Clocks must not feed data inputs of flip-flops.

Correcting a Rule Violation

- All clocks must be controlled from PIs.

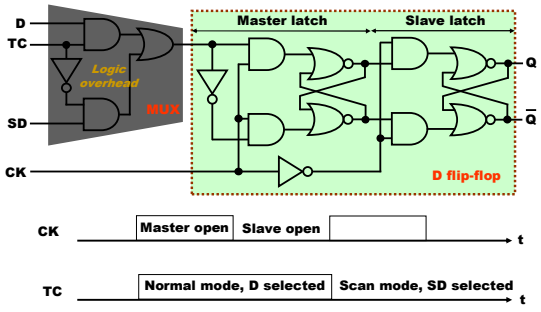


Correcting a Rule Violation

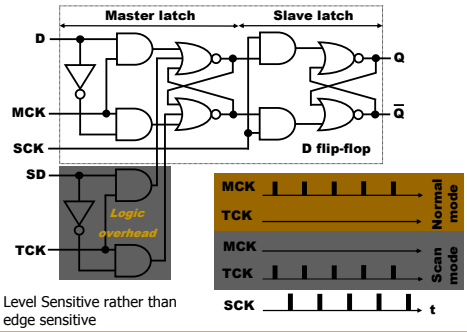


D Flip-Flop Scan Flip-Flop

Scan Flip-Flop (Master-Slave)

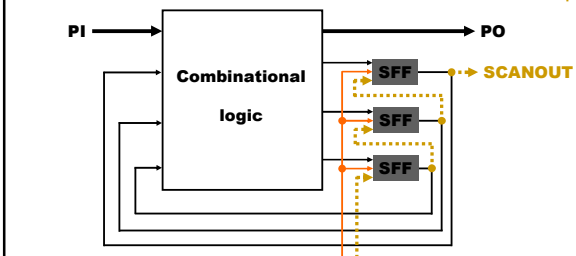


Level-Sensitive Scan-Design Latch (LSSD)



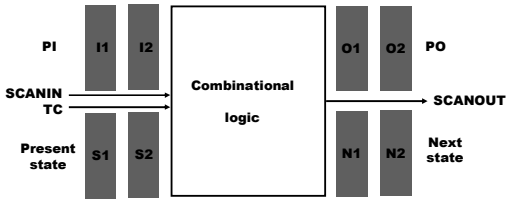
Level Sensitive rather than edge sensitive

Adding Scan Structure

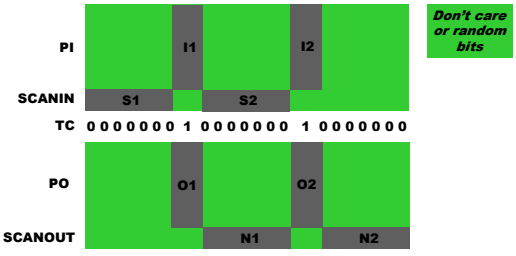


Scan Path
Also called Scan Chain

Comb. Test Vectors



Comb. Test Vectors



Sequence length = $(n_{sff} + 1)\, n_{comb} + n_{sff}$ *clock periods*

n_{comb} = number of combinational vectors

n_{sff} = number of scan flip-flops

Testing Scan Register

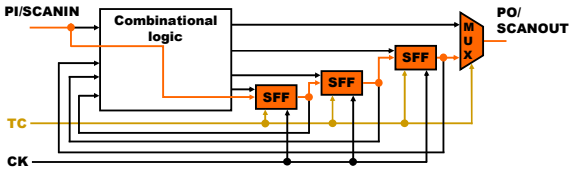
- Scan register must be tested prior to application of scan test sequences.
- A shift sequence 00110011 . . . of length $n_{sff}+4$ in scan mode (TC=0) produces 00, 01, 11 and 10 transitions in all flip-flops and observes the result at SCANOUT output.
- Total scan test length:

  $((n_{sff} + 1)\, n_{comb} + n_{sff}\,) + (n_{sff} + 4)$ *clock periods*.

  $(n_{comb} + 2)\, n_{sff} + n_{comb} + 4$ *clock periods*.
- Example: 2,000 scan flip-flops, 500 comb. vectors, total scan test length ~ 10^6 clocks.
- Multiple scan registers reduce test length.

Multiple Scan Registers

- Scan flip-flops can be distributed among any number of shift registers, each having a separate *scanin* and *scanout* pin.
- Test sequence length is determined by the longest scan shift register.
- Just one *test control* (TC) pin is essential.



Multiple Scan Registers

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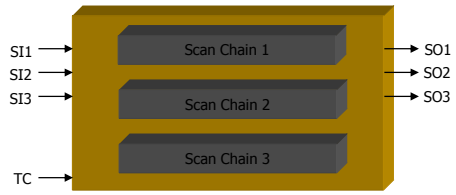


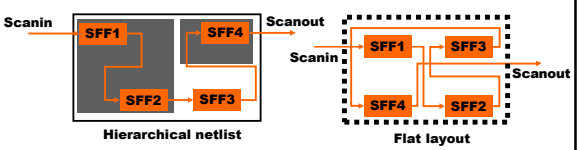
Scan Overhead

- IO pins: One pin necessary.
- Area overhead:
  - *Gate overhead* = $[4\, n_{sff}/(n_g+10n_{ff})]$ x 100%,

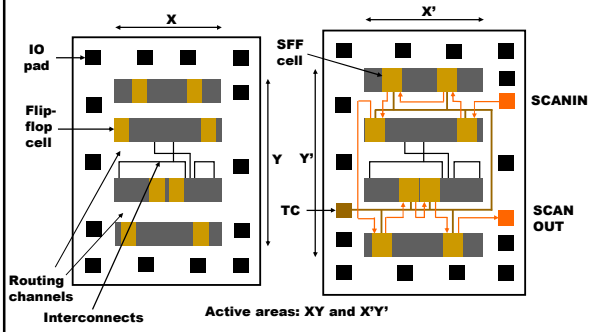
    where n_g = *comb. gates*; n_{ff} = *flip-flops*;
    - Example – n_g = 100k gates, n_{ff} = 2k *flip-flops*, overhead = 6.7%.
  - More accurate estimate must consider scan wiring and layout area.
- Performance overhead:
  - Multiplexer delay added in combinational path; approx. two gate-delays.
  - Flip-flop output loading due to one additional fanout; approx. 5-6%.

Hierarchical Scan

- Scan flip-flops are chained within subnetworks before chaining subnetworks.
- Advantages:
  - Automatic scan insertion in netlist
  - Circuit hierarchy preserved – helps in debugging and design changes
- Disadvantage: Non-optimum chip layout.



Optimum Scan Layout



Scan Area Overhead

Linear dimensions of active area:

$X = (C + S) / r$

$X' = (C + S + \alpha S) / r$

$Y' = Y + ry = Y + Y(1-\beta) / T$

Area overhead

$$= \frac{X'Y' - XY}{XY} \times 100\%$$

$$= \left[(1+\alpha s)\left(1+\frac{1-\beta}{T}\right) - 1\right] \times 100\%$$

$$= \left(\alpha s + \frac{1-\beta}{T}\right) \times 100\%$$

y = track dimension, wire width+separation
C = total comb. cell width
S = total non-scan FF cell width
s = fractional FF cell area = S/(C+S)
α = SFF cell width fractional increase
r = number of cell rows or routing channels
β = routing fraction in active area
T = cell height in track dimension y

Example: Scan Layout

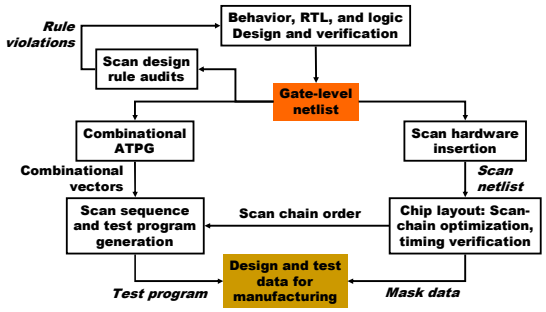
- 2,000-gate CMOS chip
- Fractional area under flip-flop cells, s = 0.478
- Scan flip-flop (SFF) cell width increase, α = 0.25
- Routing area fraction, β = 0.471
- Cell height in routing tracks, T = 10
- Calculated overhead = 17.24%
- Actual measured data and performance:

Scan implementation	Area overhead	Normalized clock rate
None	0.0	1.00
Hierarchical	16.93%	0.87
Optimum layout	11.90%	0.91

ATPG Example: S5378

	Sequential ATPG Original	Full-scan
Number of combinational gates	2,781	2,781
Number of non-scan flip-flops (10 gates each)	179	0
Number of scan flip-flops (14 gates each)	0	179
Gate overhead	0.0%	15.66%
Number of faults	4,603	4,603
PI/PO for ATPG	35/49	214/228
Fault coverage	70.0%	99.1%
Fault efficiency	70.9%	100.0%
CPU time on SUN Ultra II, 200MHz processor	5,533 s	5 s
Number of ATPG vectors	414	585
Scan sequence length	414	105,662

Automated Scan Design



Timing and Power

- Small delays in scan path and clock skew can cause race condition.
- Large delays in scan path require slower scan clock.
- Dynamic multiplexers: Skew between TC and TC signals can cause momentary shorting of D and SD inputs.
- Random signal activity in combinational circuit during scan can cause excessive power dissipation.

Summary

- Scan is the most popular DFT technique:
  - Rule-based design
  - Automated DFT hardware insertion
  - Combinational ATPG
- Advantages:
  - Design automation
  - High fault coverage; helpful in diagnosis
  - Hierarchical – scan-testable modules are easily combined into large scan-testable systems
  - Moderate area (~10%) and speed (~5%) overhead
- Disadvantages:
  - Large test data volume and long test time
  - Basically a slow speed (DC) test