VLSI Design Verification and Testing

Logic and Fault Modeling

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Overview

- Motivation
- Logic Modeling
  - Model types
  - Models at different levels of abstractions
  - Models and definitions
- Fault Modeling
  - Why model faults?
  - Some real defects in VLSI and PCB
  - Common fault models
  - Stuck-at faults
    - Single stuck-at faults
    - Multiple stuck-at faults
  - Transistor faults

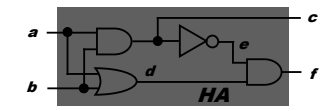
Motivation

- Models are often easier to work with
- Models are portable
- Models can be used for simulation, thus avoiding expensive hardware/actual circuit implementation
- Nearly all engineering systems are studied using models
- All the above apply for logic as well as for fault modeling

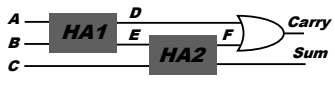
Logic Modeling – Model types

- **Behavior**
  - **System at I/O level**
  - **Timing info provided**
  - **Internal details missing**
- **Functional**
  - **DC behavior – no timing**
- **Structural**
  - **Gate level description**
    - Models are often described using a hierarchy

Hierarchical Model: A Full-Adder



HA;
inputs: a, b;
outputs: c, f;
AND: A1, (a, b), (c);
AND: A2, (d, e), (f);
OR: O1, (a, b), (d);
NOT: N1, (c), (e);



FA;
inputs: A, B, C;
outputs: Carry, Sum;
HA: HA1, (A, B), (D, E);
HA: HA2, (E, C), (F, Sum);
OR: O2, (D, F), (Carry);

Modeling Levels

Modeling level	Circuit description	Signal values	Timing	Application
Function, behavior, RTL	Programming language-like HDL	0, 1	Clock boundary	Architectural and functional verification
Logic	Connectivity of Boolean gates, flip-flops and transistors	0, 1, X and Z	Zero-delay unit-delay, multiple-delay	Logic verification and test
Switch	Transistor size and connectivity, node capacitances	0, 1 and X	Zero-delay	Logic verification
Timing	Transistor technology data, connectivity, node capacitances	Analog voltage	Fine-grain timing	Timing verification
Circuit	Tech. Data, active/ passive component connectivity	Analog voltage, current	Continuous time	Digital timing and analog circuit verification

Logic Models and Definitions

- **Program model of a circuit**
  - **Express circuit (gate level) as a program consisting of interconnected logic operations**
  - **Execute the program to determine circuit output for varying inputs**
- **RTL model**
  - **Higher level model of the circuit**
- **HDL model**
  - **Examples at this level are verilog HDL and VHDL**

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Logic Models and Definitions

- **Structural model**
  - **External representation in the form of netlist**
  - **Examples of this are uw format, iscas format, EDIF, …**
  - **Some keyword used in such representation**
    - **Primary inputs and Primary outputs**
    - **Gates: AND, OR, NOT, …**
    - **Storage: latch, flip-flop**
    - **Connections: lines, nets**
    - **Fanin: number of inputs to a gate**
    - **Fanout: number of lines a signal feeds**
    - **Fanout-free circuit: every line or gate has a fanout of one**

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netlist Format: Two Examples

ISCAS Benchmarks: http://www.fm.vslib.cz/~kes/asic/iscas/

uw format

```
#  gate  connected to
1   PI    4, 5;
2   PO    3, 6;
3  not    5;
4  not    6;
5  and    7;
6  and    7;
7   or;
7   PO
```

iscas format (comb.)

```
#  gate  #outputs  # inputs
    input gate #
1   input   2  0
8   fanoutfrom   1
9   fanoutfrom   1
2   input   2  0
10 fanoutfrom  2
11 fanoutfrom  2
3   not     1    1
      11
4   not     1    1
      9
5   and     1    2
      3    8
6   and     1    2
      4    10
7   or      1    2
      5    6
7   output
```

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Logic Models and definitions

- Additional useful terms
  - Graph representation
  - Reconvergent fanouts
  - Stems and branches
  - Logic levels in a circuit
  - "levelization" of a circuit

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Fault Modeling

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Why Model Faults?

- **I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing)**
- **Real defects (often mechanical) too numerous and often not analyzable**
- **A fault model identifies targets for testing**
- **A fault model makes analysis possible**
- **Effectiveness measurable by experiments**

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Some Real Defects in Chips

- Processing defects
  - Missing contact windows
  - Parasitic transistors
  - Oxide breakdown
  - . . .
- Material defects
  - Bulk defects (cracks, crystal imperfections)
  - Surface impurities (ion migration)
  - . . .
- Time-dependent failures (Age defects)
  - Dielectric breakdown
  - Electromigration
  - . . .
- Packaging failures
  - Contact degradation
  - Seal leaks
  - . . .

Ref.: M. J. Howes and D. V. Morgan, *Reliability and Degradation - Semiconductor Devices and Circuits*, Wiley, 1981.

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FMA

- Defects occur either during manufacture or during the use of device.
- Repeated occurrence of the same defects indicates the need for improvements in the manufacturing process or design of the device.
- Procedures for diagnosing defects and finding their causes are known as failure mode analysis (FMA).

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Defect, Fault, and Error

- **Defect** (imperfection in hardware):
  - A defect in an electronic system is the unintended difference between the implemented hardware and its intended design.
- **Error:**
  - A wrong output signal produced by a defective system is called an error. An error is an "effect" whose cause is some "defect".
- **Fault** (imperfection in function):
  - A representation of a "defect" at the abstracted function level is called a fault.

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Observed PCB Defects

Defect classes	Occurrence frequency (%)
Shorts	51
Opens	1
Missing components	6
Wrong components	13
Reversed components	6
Bent leads	8
Analog specifications	5
Digital logic	5
Performance (timing)	5

Ref.: J. Bateson, *In-Circuit Testing*, Van Nostrand Reinhold, 1985.

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Common Fault Models

- Single stuck-at faults
- Transistor open and short faults
- Memory faults
- PLA faults (stuck-at, cross-point, bridging)
- Functional faults (processors)
- Delay faults (transition, path)
- Analog faults
- For more examples, see Section 4.4 (p. 60-70) of the book.

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Stuck-at Faults

- Single stuck-at faults
- What does it achieve in practice?
- Fault equivalence
- Fault dominance and checkpoint theorem
- Classes of stuck-at faults and multiple faults

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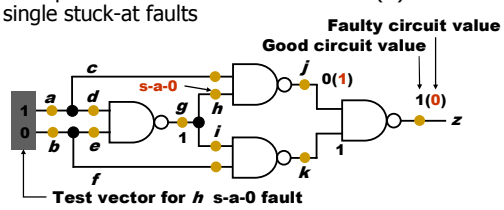
Single Stuck-at Fault

- Three properties define a single stuck-at fault
  - Only one line is faulty
  - The faulty line is *permanently* set to 0 or 1
  - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults



Single Stuck-at Faults (contd.)

- **How effective is this model?**
  - **Empirical evidence supports the use of this model**
  - **Has been found to be effective to detect other types of faults**
  - **Relates to yield modeling**
  - **Simple to use**

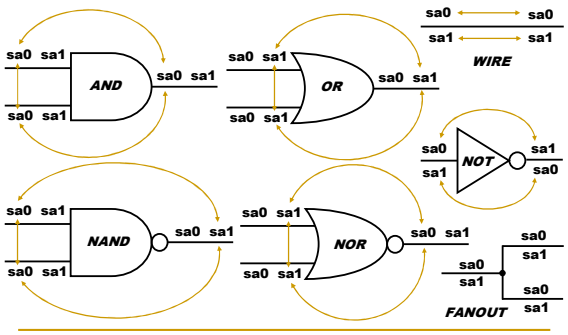
Why Not Multiple Stuck-at Faults

- **In general, several stuck-at faults can be simultaneously present in the circuit.**
- **A circuit with n lines can have 3^n-1 possible stuck line combinations.**
  - **There are three states: s-a-1, s-a-0, and fault-free**
- **Even a moderate value n will give an enormously large number of multiple stuck-at faults.**
- **It's a common practice to model only single stuck-at faults.**
  - **A n-line circuit can have at most 2n single stuck-at faults.**
  - **This number is further reduced by techniques known as Fault Collapsing.**

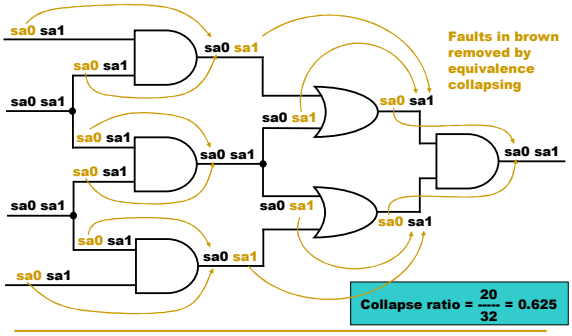
Fault Equivalence

- **Number of fault sites in a Boolean gate circuit = #PI + #gates + # (fanout branches).**
- **Fault equivalence:**
  - **Two faults f1 and f2 are equivalent if all tests that detect f1 also detect f2.**
  - **If faults f1 and f2 are equivalent then the corresponding faulty functions are identical.**
- **Fault collapsing:**
  - **All single faults of a logic circuit can be divided into disjoint equivalence subsets, where all faults in a subset are mutually equivalent. A collapsed fault set contains one fault from each equivalence subset.**

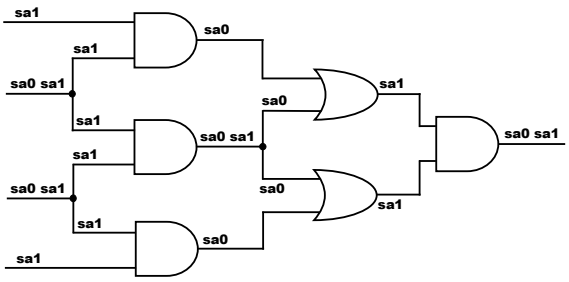
Equivalence Rules



Equivalence Example



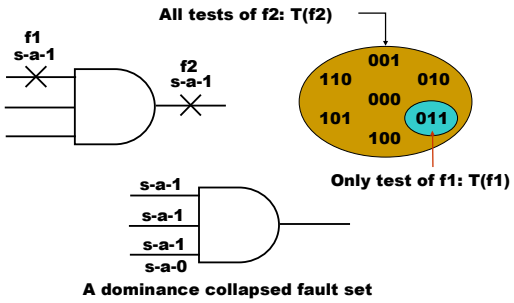
Equivalence Example



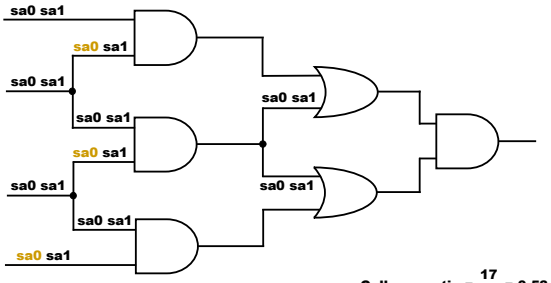
Fault Dominance

- If all tests of some fault f1 detect another fault f2, then f2 is said to dominate f1.
- Dominance fault collapsing:
  - If fault f2 dominates f1, then f2 is removed from the fault list.
  - When dominance fault collapsing is used, it is sufficient to consider only the input faults of Boolean gates.
  - See the next example.
- In a tree circuit (without fanouts) PI faults form a dominance collapsed fault set.
- If two faults dominate each other then they are equivalent.

Dominance Example

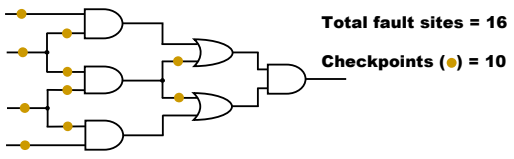


Dominance Example



Checkpoints

- Primary inputs and fanout branches of a combinational circuit are called *checkpoints*.
- Checkpoint theorem: A test set that detects all single (multiple) stuck-at faults on all checkpoints of a combinational circuit, also detects all single (multiple) stuck-at faults in that circuit.



Classes of Stuck-at Faults

- Following classes of single stuck-at faults are identified by fault simulators:
  - Potentially-detectable fault -- Test produces an unknown (X) state at primary output (PO); detection is probabilistic, usually with 50% probability.
  - Initialization fault -- Fault prevents initialization of the faulty circuit; can be detected as a potentially-detectable fault.
  - Hyperactive fault -- Fault induces much internal signal activity without reaching PO.
  - Redundant fault -- No test exists for the fault.
  - Untestable fault -- Test generator is unable to find a test.

Multiple Stuck-at Faults

- A multiple stuck-at fault means that any set of lines is stuck-at some combination of (0,1) values.
- The total number of single and multiple stuck-at faults in a circuit with n single fault sites is 3^n-1.
- A single fault test can fail to detect the target fault if another fault is also present, however, such masking of one fault by another is rare.
- Statistically, single fault tests cover a very large number of multiple faults.

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Transistor (Switch) Faults

- MOS transistor is considered an ideal switch and two types of faults are modeled:
  - **Stuck-open** -- a single transistor is permanently stuck in the open state.
  - **Stuck-short** -- a single transistor is permanently shorted irrespective of its gate voltage.
- Detection of a stuck-open fault requires two vectors (V1 and V2).
- Detection of a stuck-short fault requires the measurement of quiescent current (I_{DDQ}).

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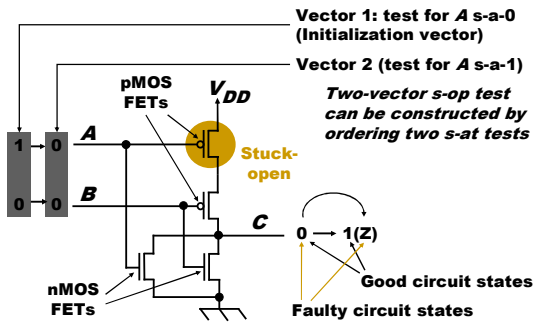
Stuck-Open Example



NOR Gate

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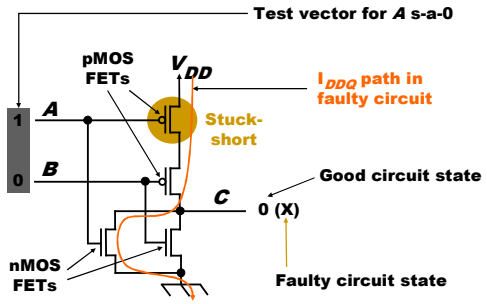
Stuck-Short Example



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