VLSI Design Verification and Testing

Test Economics and Product Quality

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Overview

- Basics of cost analysis
- Economics of DFT
- VLSI chip Yield
- VLSI defects – clustered and unclustured
- Yield equations
- Defect, Yield, and Coverage
- Parameter estimation
- Economics

Motivation

- Impact of testing or not testing on the cost of final product
  - Study basics of economics
  - How testing related to the product
  - How lack of testing can affect the quality and the product cost

Basics of cost analysis

- **There are several types of costs:**
  - **Fixed cost**
  - **Variable cost**
  - **Total cost**
  - **Average cost**

Example: ***Costs of running a car***

Fixed cost	**$25,000**	**Purchase price of car**
Variable cost	**~~20~~ cents/mile**	**Gasoline, maintenance, repairs**
Total cost	**$25,000 + 0.2*x***	**For traveling *x* miles**
Average cost	**$ 25,000 / *x* + 0.2**	**Total cost / *x***

Simple Cost Analysis

Case 1: 10,000 miles/yr, $12,500 resale value after 5 years

$$\text{Average cost} = \$ \frac{25,000 - 12,500}{50,000} + 0.2 = 45 \text{ cents/mile}$$

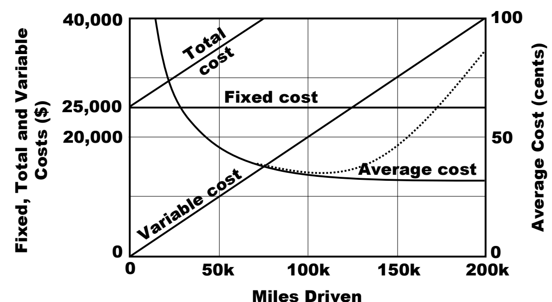
Case 2: 10,000 miles/yr, $6,250 resale value after 10 years

$$\text{Average cost} = \$ \frac{25,000 - 6,250}{100,000} + 0.2 = 38.75 \text{ cents/mile}$$

Case 3: 10,000 miles/yr, $0 resale value after 20 years

$$\text{Average cost} = \$ \frac{25,000 - 0}{200,000} + 0.2 = 32.5 \text{ cents/mile}$$

Cost Analysis Graph



Production

- **Inputs to production (*x- cost*): Labor, land, capital, enterprise, energy (*x* may include both fixed and variable costs)**
- **Production output - product as a function of input *Q = f (x)***
- **Average product: product per unit input - *Q / x***
- **Marginal product** - *dQ / dx*

Benefit-Cost Analysis

- **Benefits:**
  - **Savings in manufacturing costs (capital and operational) and time, reduced wastage, automation, etc.**
- **Costs:**
  - **Extra hardware, training of personnel, etc.**
- **Benefit/cost ratio**

$$\text{B/C ratio} = \frac{\text{Annual benefits}}{\text{Annual costs}} > 1$$

Economics of Design for Testability (DFT)

- **Consider life-cycle cost; DFT on chip may impact the costs at board and system levels.**
- **Weigh costs against benefits**
  - **<u>Cost examples:</u> reduced yield due to area overhead, yield loss due to non-functional tests**
  - **<u>Benefit examples:</u> Reduced ATE cost due to self-test, inexpensive alternatives to burn-in test, increased fault/defect coverage**

Benefits and Costs of DFT

Level	Design and test	Fabri- cation	Manuf. Test	Maintenance test	Diagnosis and repair	Service interruption
Chips	+ / -	+	-			
Boards	+ / -	+	-		-	
System	+ / -	+	-	-	-	-

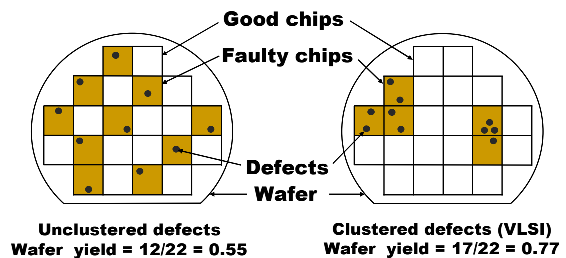
\+ Cost increase
\- Cost saving
+/- Cost increase may balance cost reduction

VLSI Chip Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.
- A chip with no manufacturing defect is called a good chip.
- Fraction (or percentage) of good chips produced in a manufacturing process is called the *yield*. Yield is denoted by symbol *Y*.
- Cost of a chip:

$$\frac{\text{Cost of fabricating and testing a wafer}}{\underbrace{\text{Yield x Number of chip sites on the wafer}}_{\text{\# Good chips on the wafer}}}$$

VLSI Defects



Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77

Yield Equation

- Chip area (A)
- Three parameters:
  - Fault density, f = average number of stuck-at faults per unit chip area
  - Fault clustering parameter, β
  - Stuck-at fault coverage, T
- Yield equation:

$$Y(T) = (1 + TAf/\beta)^{-\beta}$$

Assuming that tests with 100% fault coverage (T=1.0) remove all faulty chips,

$$Y = Y(1) = (1 + Af/\beta)^{-\beta}$$

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Defect, Yield, and Coverage

- *Defect level* (DL) is the ratio of faulty chips among the chips that pass tests.
  - Aka Escape
- DL is measured as *parts per million* (ppm).
  - Defective parts per million (DPPM)
- DL is a measure of the effectiveness of tests.
- DL is a quantitative measure of the manufactured product quality. For commercial VLSI chips a DL greater than 500 ppm is considered unacceptable.

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Determination of DL

- From field return data:
  - Chips failing in the field are returned to the manufacturer. The number of returned chips normalized to one million chips shipped is the DL.
- From test data:
  - Fault coverage of tests and chip fallout rate are analyzed. A modified yield model is fitted to the fallout data to estimate the DL.
  - Chip fallout: Fraction of chips failing up to a vector in the test set

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Defect Level

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)}$$

$$= 1 - \frac{(\beta + TAf)^{\beta}}{(\beta + Af)^{\beta}}$$

Where T is the fault coverage of tests, Af is the average number of faults on the chip of area A, β is the fault clustering parameter. Af and β are determined by test data analysis.

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Defect Level (2)

An alternative equation relating DL, Yield, and fault-coverage, in case of unclustered random defects is:

$$DL(T) = 1 - Y^{1-T}$$

Where T is the fault coverage of tests.

Note that Y is the ratios of the "devices tested good" to the "total number of devices tested or fabricated/manufactured"

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Example: SEMATECH Chip

- "Bus interface controller ASIC" fabricated and tested at IBM, Burlington, Vermont
- 116,000 equivalent (2-input NAND) gates
- 304-pin package, 249 I/O
- Clock: 40MHz, some parts 50MHz
- 0.45µ CMOS, 3.3V, 9.4mm x 8.8mm area
- Full scan, 99.79% fault coverage
- Advantest 3381 ATE
- Data obtained courtesy of Phil Nigh (IBM)

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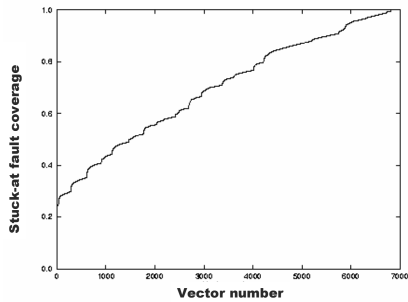
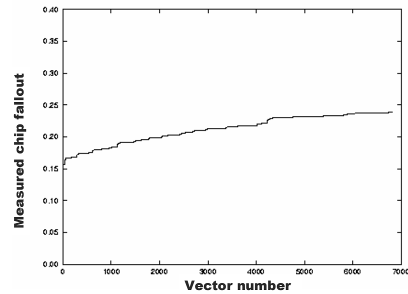
Test Coverage from Fault Simulator

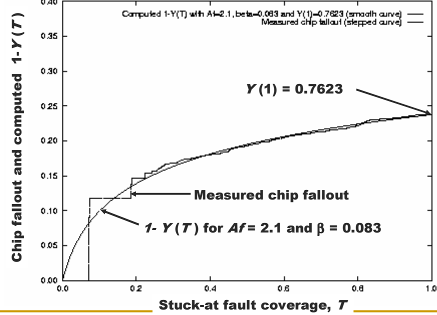


Measured Chip Fallout (18,466 chips, Y=76%)

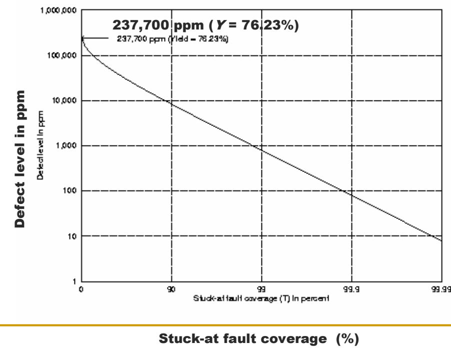
- Chip fallout: Fraction of chips failing up to a vector in the test set



Model Fitting



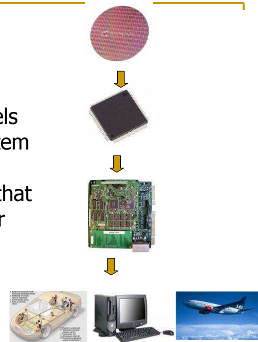
Computed DL



Economics – impact at higher levels

Rule of 10 – A reminder

- A device that needs to be tested at higher level (levels being: Chip – board – system – system in field) costs 10 time (and possibly more) that of cost of testing it a lower level



Economics – impact at higher levels

An example to demonstrate the impact of defects at system level

- Probability an IC is "bad" - p_{bad}
- A board uses *n* such ICs
- Probability of the board being "good" = $(1-p_{bad})^n$
- Consider a board with 40 devices and
  Y = 0.75, T = 0.9
- Now consider the case when T is increased to 0.99 while keeping the Yield same as 75%

Summary

- VLSI yield depends on two process parameters, fault density (*f*) and clustering parameter (β)
- Yield drops as chip area increases; low yield means high cost
- Fault coverage measures the test quality
- Defect level (DL) or reject ratio is a measure of chip quality
- DL can be determined by an analysis of test data
- For high quality: DL < 500 ppm, fault coverage ~ 99%
- DL and Yield have a major impact on the cost and quality at higher level