

VLSI Design Verification and Testing

VLSI Testing

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Objective

- Need to understand
 - Types of tests performed at different stages
 - Verification Testing
 - Manufacturing Testing
 - Acceptance Testing
 - *Automatic Test Equipment* (ATE) technology
 - Influences what tests are possible
 - Measurement limitations
 - Impact on cost
 - Parametric test

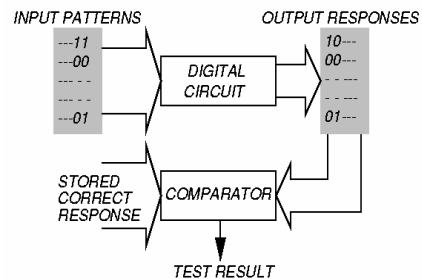
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Types of Testing

- *Testing principle*
 - Apply inputs and compare "outputs" with the "expected outputs"
- *Verification testing, or design debug*
 - Verifies correctness of design and of test procedure
 - usually requires correction to design
- *Characterization testing*
 - Used to characterize devices and performed through production life to improve the process, hence yield
- *Manufacturing testing*
 - Factory testing of all manufactured chips for parametric faults and for random defects
- *Acceptance testing (incoming inspection)*
 - User (customer) tests purchased parts to ensure quality

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Testing Principle



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Verification Testing

- Ferociously expensive
- Often a software approach
- But, may comprise:
 - Scanning Electron Microscope tests
 - Bright-Lite detection of defects
 - Electron beam testing
 - Artificial intelligence (expert system) methods
 - Repeated functional tests

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Characterization Test

- aka design debug or verification testing
- Use of test structures
 - Special structures, placed on a wafer at strategic locations, are tested to characterize the process or to determine if testing of chips should proceed
- Worst-case test
 - Choose test that passes/fails chips
 - Select statistically significant sample of chips
 - Repeat test for combination of 2+ environmental variables
 - Plot results in *Schmoo plot*
 - Diagnose and correct design errors
- Continue throughout production life of chips
 - Improve design and process to increase yield
 - Characterization may be done for the chips rejected during the production test

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Manufacturing Test

(Also called **production test**)

- Determines if manufactured chip meets specs
- Must cover high % of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis
- Go/no-go decision is made
- Tests every device on chip
- Tests are functional or at speed of application or speed guaranteed by supplier

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Burn-in or Stress Test

- Process:
 - Subject chips to high temperature & over-voltage supply, while running production tests
- Catches:
 - *Infant mortality* cases – these are damaged chips that will fail in the first 2 days of operation – causes bad devices to actually fail before chips are shipped to customers
 - *Freak failures* – devices having same failure mechanisms as reliable devices

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Types of Manufacturing Tests

- *Wafer sort* or *probe* test – done before wafer is scribed and cut into chips
 - Includes test site characterization – specific test devices are checked with specific patterns to measure:
 - Gate threshold
 - Gate delays
 - Polysilicon field threshold
 - Poly sheet resistance, etc.
- Packaged device tests

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Sub-types of Tests

- Parametric Tests:
 - measures electrical properties of pin electronics – delay, voltages, currents, etc. – fast and cheap.
- Functional Tests:
 - used to cover very high % of modeled faults – test every transistor and wire in digital circuits – long and expensive.
 - the focus of this course

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Two Different Meanings of Functional Test

- *ATE and Manufacturing World*
 - any vectors applied to cover high % of faults during manufacturing test
- *Automatic Test-Pattern Generation World*
 - testing with verification vectors or vectors generated without structural information, which determine whether hardware matches its specification – typically have low fault coverage (< 70 %)

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Incoming Inspection

- Can be:
 - Similar to production testing
 - More comprehensive than production testing
 - Test time may not be an issue
 - Tuned to specific systems application
- Often done for a random sample of devices
 - *Sample size* depends on device quality and system reliability requirements
 - Avoids putting defective device in a system where cost of diagnosis exceeds incoming inspection cost

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Automatic Test Equipment (ATE)

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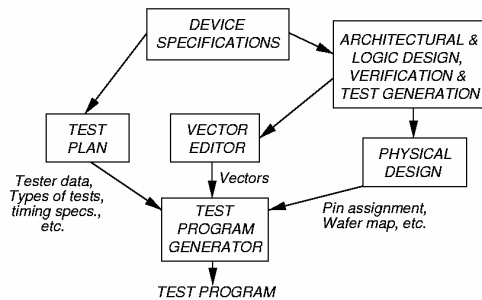
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Test Specifications & Plan

- Test Specifications:
 - Functional Characteristics
 - Type of Device Under Test (DUT), Logic, Memory, uP
 - Physical Constraints – Package, pin numbers, etc.
 - Environmental Characteristics – supply, temperature, humidity, etc.
 - Reliability – acceptance quality level (defects/million), failure rate, etc.
- Test plan generated from specifications
 - Type of test equipment to use
 - Types of tests
 - Fault coverage requirement

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Test Programming



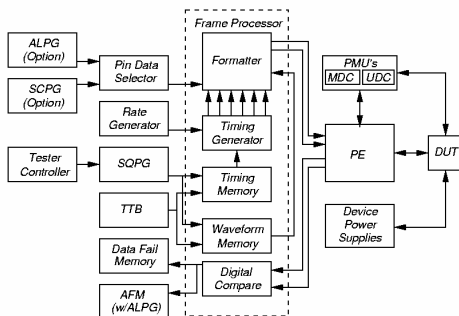
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ADVANTEST Model T6682 ATE



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T6682 ATE Block Diagram



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T6682 ATE Specifications

- Uses 0.35 μm VLSI chips in implementation
- 1024 pin channels
- Speed: 250, 500, or 1000 MHz
- Timing accuracy: +/- 200 ps
- Drive voltage: -2.5 to 6 V
- Clock/strobe accuracy: +/- 870 ps
- Clock settling resolution: 31.25 ps
- Pattern multiplexing:
 - write 2 patterns in one ATE cycle
- Pin multiplexing:
 - use 2 pins to control 1 DUT pin

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Pattern Generation

- Sequential pattern generator (SQPG):
 - stores 16 Mvectors of patterns to apply to DUT, vector width determined by # DUT pins
- Algorithmic pattern generator (ALPG): 32 independent address bits, 36 data bits
 - For memory test – has address descrambler
 - Has address failure memory
- Scan pattern generator (SCPG) supports JTAG boundary scan, greatly reduces test vector memory for full-scan testing
 - 2 Gvector or 8 Gvector sizes

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Response Checking and Frame Processor

- Response Checking:
 - Pulse train matching – ATE matches patterns on 1 pin for up to 16 cycles
 - Pattern matching mode – matches pattern on a number of pins in 1 cycle
 - Determines whether DUT output is correct, changes patterns in real time
- Frame Processor:
 - combines DUT input stimulus from pattern generators with DUT output waveform comparison
- Strobe time:
 - interval after pattern application when outputs sampled

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Probing

- Pin electronics (PE) – electrical buffering circuits, put as close as possible to DUT
- Uses pogo pin connector at test head
- Test head interface through custom printed circuit board to wafer prober (unpackaged chip test) or package handler (packaged chip test), touches chips through a socket (contactor)
- Uses liquid cooling
- Can independently set V_{IH} , V_{IL} , V_{OH} , V_{OL} , I_H , I_L , V_T for each pin
- Parametric Measurement Unit (PMU)

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Test Data Analysis

- Uses of ATE test data:
 - Reject bad DUTS
 - Fabrication process information
 - Design weakness information
- Devices that did not fail are good only if tests covered 100% of faults
- *Failure mode analysis* (FMA)
 - Diagnose reasons for device failure, and find design and process weaknesses
 - Allows improvement of logic & layout design rules

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Probe Card and Probe Needles or Membrane

- Probe card:
 - custom printed circuit board (PCB) on which DUT is mounted in socket – may contain custom measurement hardware (current test)
- Probe needles:
 - come down and scratch the pads to stimulate/read pins
- Membrane probe:
 - for unpackaged wafers – contacts printed on flexible membrane, pulled down onto wafer with compressed air to get wiping action

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T6682 ATE Software

- Runs Solaris UNIX on UltraSPARC 167 MHz CPU for non-real time functions
- Runs real-time OS on UltraSPARC 200 MHz CPU for tester control
- Peripherals: disk, CD-ROM, micro-floppy, monitor, keyboard, HP GPIB, Ethernet
- *Viewpoint* software provided to debug, evaluate, & analyze VLSI chips

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Multi-site Testing – Major Cost Reduction

- One ATE tests several (usually identical) devices at the same time
- For both probe and package test
- DUT interface board has > 1 sockets
- Add more instruments to ATE to handle multiple devices simultaneously
- Usually test 2 or 4 DUTs at a time, usually test 32 or 64 memory chips at a time
- Limits: # instruments available in ATE, type of handling equipment available for package

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Electrical Parametric Testing

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Electrical Parametric Testing

Typical tests

DC parametric test

- Probe test (wafer sort) – catches gross defects
- Contact, power, open, short tests
- Functional & layout-related test

AC parametric test

- Unacceptable voltage/current/delay at pin
- Unacceptable device operation limits

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DC Parametric Tests

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Contact Test

-- Verifies that the chip pins have no opens or shorts

1. Set all inputs to 0 V
2. Force current I_{fb} out of pin (expect I_{fb} to be 100 to 250 μ A)
3. Measure pin voltage V_{pin} . Calculate pin resistance R
 - Contact short ($R = 0 \Omega$)
 - No problem
 - Pin open circuited (R huge), I_{fb} and V_{pin} large

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Power Consumption Test

Finds the worst case power consumption for static (steady input logic values) and dynamic (inputs changing dynamically during operation) situations.

1. Set temperature to worst case, open circuit DUT outputs
2. Measure maximum device current drawn from supply I_{CC} at specified voltage
 - $I_{CC} > 70$ mA (fails)
 - 40 mA $< I_{CC} \leq 70$ mA (ok)

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Output Short Current Test

This test verifies that the output current drive is sustained at high and low output voltages.

1. Make chip output a 1
2. Short output pin to 0 V in PMU
3. Measure short current (but not for long, or the pin driver burns out)
 - ❑ Short current $> 40 \mu\text{A}$ (ok)
 - ❑ Short current $\leq 40 \mu\text{A}$ (fails)

PMU: Parametric measurement unit

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Output Drive Current Test

For a specified output drive current, this test verifies that the output voltage is maintained.

1. Apply vector forcing pin to 0
2. Simultaneously force V_{OL} (0.4V) voltage and measure I_{OL}
3. Repeat Step 2 for logic 1
 - ❑ $I_{OL} < 2.1 \text{ mA}$ (fails)
 - ❑ $I_{OH} < -1 \text{ mA}$ (fails)

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Threshold Test

This determines the V_{IL} and V_{IH} input voltages needed to cause the device to switch from high to low (low to high). $0 < V_{OL} < V_{IL} < V_{IH} < V_{OH} < V_{CC}$.

1. For each I/P pin, write logic 0 followed by propagation pattern to output. Read output. Increase input voltage in 0.1 V steps until output value is wrong
2. Repeat process, but stepping down from logic 1 by 0.1 V until output value fails
 - ❑ Wrong output when 0 input $> 0.8 \text{ V}$ (ok)
 - ❑ Wrong output when 0 input $\leq 0.8 \text{ V}$ (fails)
 - ❑ Wrong output when 1 input $< 2.0 \text{ V}$ (ok)
 - ❑ Wrong output when 1 input $\geq 2.0 \text{ V}$ (fails)

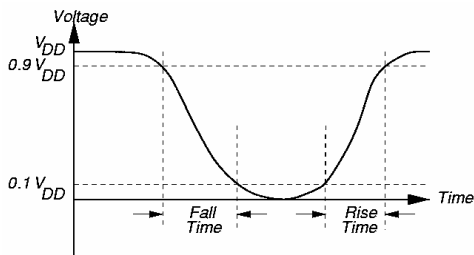
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AC Parametric Tests

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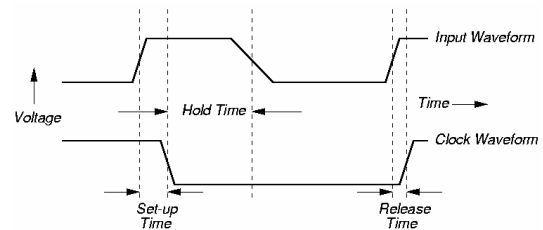
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Rise/fall Time Tests



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Set-up and Hold Time Tests



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Propagation Delay Tests

1. Apply standard output pin load (*RC* or *RL*)
 2. Apply input pulse with specific rise/fall
 3. Measure propagation delay from input to output
 - Delay between 5 ns and 40 ns (ok)
 - Delay outside range (fails)
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