VLSI Design Verification and Testing

Introduction

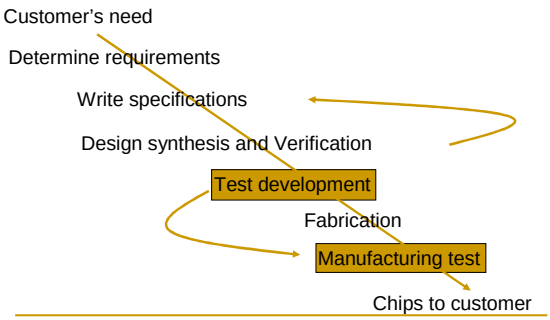
Mohammad Tehranipoor

Electrical and Computer Engineering
University of Connecticut

Course Outline

- Course outline
  - Part I: Introduction to VLSI testing
  - Part II: Test methods
  - Part III: Design for testability

VLSI Realization Process



Present and Future*

	1997-2001	2003-2006	2009-2012
Feature size (micron)	0.25 - 0.15	0.13 - 0.10	0.07-0.05
Transistors/cm²	4 - 10M	18 - 39M	84-180
Pin count	100 - 900	160 - 1475	260-2690
Clock rate (MHz)	200 - 730	530 - 1100	840-1830
Power (Watts)	1.2 - 61	2 - 96	2.8-109

*** SIA Roadmap, *IEEE Spectrum*, July 1999**

ITRS

Present and Future

- What is happening to the test cost
  - Automatic Test Equipment (ATE) cost
  - Test time
  - Escape
  - Yield loss
- Compression
- At-speed testing
- New subtle defects
- Power delivery issue
  - Source: IEEE D&T, Jan 2000

Contract between design house and fab vendor

- Design is complete and checked (verified)
- Fab vendor: How will you test it?
- Design house: I have checked it and …
- Fab vendor: But, how would you test it?
- Design house: Why is that important?
- *complete the story*

- That is one reason for design-for-testability, test generation etc.

Contract between design …

Hence:
- "Test" must be comprehensive
- It must not be "too long"

Issues:
- Model possible defects in the process
  - Understand the process
- Develop simulator and fault simulator
- Develop test generator
- Methods to quantify the test efficiency
  - Fault coverage

Verification v/s Testing

Definitions

- Design synthesis:
  - Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification:
  - Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test:
  - A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

Verification v/s Testing

Verification	Testing
Verifies correctness of design.	Verifies correctness of manufactured hardware.
Performed by simulation, hardware emulation, or formal methods.	Two-part process: 1. Test generation: software process executed once during design 2. Test application: electrical tests applied to hardware
Performed once prior to manufacturing.	Test application performed on "**every**" manufactured device.
Responsible for quality of design.	Responsible for quality of devices.

Need for testing

- Functionality issue
  - Does the circuit (large or small) work?
- Density issue
  - Higher density ⇒ higher failure prob
- Application issue
  - Life critical applications
- Maintenance issue
  - Need to identify failed components
- Cost of doing business
- What does testing achieve?
  - Discard only the "bad product"?

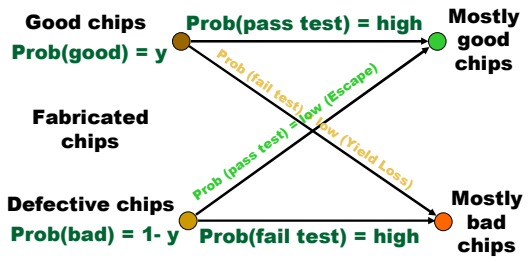
Ideal Tests

- Ideal tests detect **all** defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

Real Tests

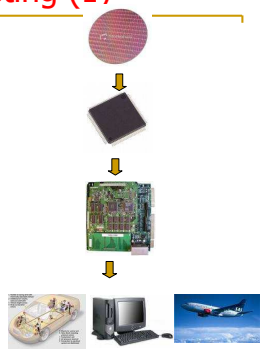
- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the **yield loss**.
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the **defect level**.

Testing as Filter Process



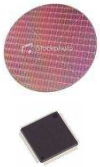
Level of testing (1)

- Levels
  - Chip
  - Board
  - System
    - Boards put together
    - System-on-Chip (SoC)
  - System in field
- Cost – Rule of 10
  - It costs 10 times more to test a device as we move to higher level in the product manufacturing process



Level of testing (2)

- Other ways to define levels – these are important to develop correct "fault models" and "simulation models"
  - Transistor
  - Gate
  - RTL
  - Functional
  - Behavioral
  - Architecture
- Focus: Chip level testing – gate level design



Costs of Testing

- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost

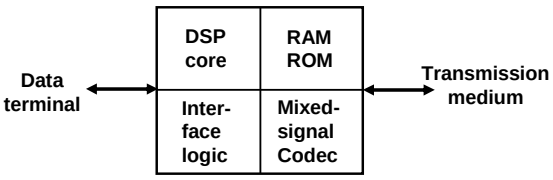
Cost of Manufacturing Test

- 0.5-1.0GHz, analog instruments,1024 digital pins: ATE purchase price
  - = $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  - = Depreciation + Maintenance + Operation
  - = $0.854M + $0.085M + $0.5M
  - = $1.439M/year
- Test cost (24 hour ATE operation)
  - = $1.439M/(365 x 24 x 3,600)
  - = 4.5 cents/second

Roles of Testing

- Detection: Determination of whether or not the *device under test* (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- Failure mode analysis (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

A Modern VLSI Device System-on-a-chip (SOC)



Emergence of SoC has made test event more challenging and expensive

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Course Outline Part I: Introduction

- Basic concepts and definitions (Chapter 1)
- Test process and ATE (Chapter 2)
- Test economics and product quality (Chapter 3)
- Fault modeling (Chapter 4)

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Course Outline (Cont.) Part II: Test Methods

- Logic and fault simulation (Chapter 5)
- Testability measures (Chapter 6)
- Combinational circuit ATPG (Chapter 7)
- Sequential circuit ATPG (Chapter 8)
- Memory test (Chapter 9)
- Delay test and IDDQ test (Chapters 12 and 13)

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Course Outline (Cont.) Part III: DFT

- Scan design (Chapter 14)
- BIST (Chapter 15)
- Boundary scan (Chapters 16)

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