Topics

- Design Strategies

Standard Cell Libraries

- How do you decide on the composition of the cell library?
  - Number of inputs
  - Transistor sizing for varying capacitive loads
  - Pullup/pulldown ratio

Compiled Cells

- Standard cells
  - Must be redesigned for every new process technology
  - Design options are limited because of discrete set of cells
  - Customized cells would provide more flexibility
    - Automatic layout generation for design-specific requirements

Automatic Cell Generation

- Compiled Cells

Cell-based Design (or standard cells)

- Macrocells
  - Hard Macros
    - Predetermined physical design
    - Fixed transistor and wiring locations
    - Dense layout, optimized performance and power characteristics
Macrocells

- Soft Macros
  - Physical design is done automatically
  - Easily ported across many different technologies and processes
  - Macro cell compiler will take a functional and parameterized description and generate a netlist of standard cells

Intellectual property

- Macrocells can be acquired from third-party vendors
  - Includes appropriate compilers, debuggers, test vectors, prediction models
  - Similar to reusable software libraries
  - Examples include embedded processors, bus interfaces, DSP processors, ECC coders, etc.
Integrating Synthesis with Physical Design

System-on-a-Chip (SoC) Design
- Embed multiple functionalities on a single chip
- SoC is a natural result of having more and more transistors available
- Managing multiple modules becomes a design challenge

System-on-a-Chip (SoC) Design
- Embedded applications
- Mixed-mode applications (Analog/Digital)
- Heavy software component
- May have programmable and application specific components

Array-Based Design
- Cell-based and fully custom designs require a run through the full manufacturing process
  - Can take up to several months before the first chip arrives
  - Mask generation costs can make it very expensive
    - As process technologies get better, the tendency has been to use more and more masks
- Alternative is array-based implementations

Array-Based Design
- Pre-diffused
  - Mask-programmable
  - Gate arrays
  - Sea of gates
- Pre-wired
  - Field programmable gate arrays (FPGA)

Gate arrays
- Uncommitted Cell
- Committed Cell (4-input NOR)
Gate arrays

- Less compact than standard cells
- Manufacturing time savings is not as significant because the design times are the most important factor now

Field Programmable Gate Arrays

- Programmable Logic Style
  - Array-based
  - Cell-based
    - Function generator
- Programming Interconnect
  - Channel-routing
  - Mesh networks

Array-Based Programmable Logic

- Lower density than custom
- Lower performance
  - Each node has significant capacitance
- Only implements combinational logic - no registers or flip-flops