Topics

- I/O
- Packaging
- Design Strategies

I/O Structures

- I/O Pads are the interface between the on-chip world and the off-chip world
- Typically 100-200µ wide
- Can consume significant amounts of power
  - 10% of power consumption on the Alpha

I/O Structures

- Output pads
  - Large drive capability
  - DC characteristics for non-CMOS loads
  - Typically staged to present lower load to internal core circuitry
- Input pads
  - Require mechanisms to prevent excessive off-chip current from damaging chip

Packaging

- Package Types
  - Pin Grid Array
  - Ball Grid Array
  - Multichip Module
- Mounting Types
  - Surface Mounted

Packaging

- Pin Grid Arrays
- Multi-Chip Modules
Packaging

- Package pins

![Package pins diagram]

Wire Bonding

- Providing electrical connection between the silicon chip and the external pins of the semiconductor device using very fine bonding wires

Solder Bump Bonding

- Pads are distributed within the chip instead of at the periphery
- Lower resistance and capacitance

Packaging

- Reliability of IC degrades as an exponential function of junction temperature
- Packaging and thermal control maintain junction temperature within allowable ranges

Packaging

- Two limits
  - Functional limit defines maximum temperature at which performance specs can be met
  - Physical limit is the maximum temperature to which device can be exposed without causing permanent damage
Power Dissipation

• Intel processor with thermal gradients

![Intel processor with thermal gradients](image)

Power Dissipation

• Pentium 4 @ 3GHz dissipates 81W
• Typical packaging dissipates 1W
  ■ That's why you need a fan!!

Design Strategies

• Design Productivity
• Design Flow
• Implementation Choices

Design Productivity Challenge

• Complexity growth of 58% per year
• Productivity growth of 21% per year

<table>
<thead>
<tr>
<th>Year</th>
<th>Transistors per chip</th>
<th>Transistors per staff-month</th>
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<tr>
<td>1981</td>
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<td>80</td>
</tr>
<tr>
<td>1991</td>
<td>50K</td>
<td>500</td>
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<td>2001</td>
<td>50M</td>
<td>5000</td>
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<td>2009</td>
<td>5B</td>
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Design Productivity Challenge

• How do you manage growth in complexity?
  ■ Improved design tools
  ■ Defined design flow
  ■ Design strategies

Implementation choices

![Implementation choices](image)
Design Methodology

- Design process traverses iteratively between three abstractions: behavior, structure, and geometry
- More and more automation for each of these steps

The Custom Approach

Custom to Automation transition

Cell-based Design (or standard cells)

Standard Cell Structure

- Fixed height
- Variable width
- VDD and GND are shared by cells in the same row
- Feedthroughs help with routing
Standard Cell Design

- Area is dominated by routing and interconnect
- Standard cell placement tools try and minimize the overall wire length

Standard Cell Design

- Newer designs have many more layers to help with routing
- Can increase density to 90% - i.e. logic cells account for 90% of chip area

Standard Cell Placement