**Topics**

- Clocking

**Synchronous Timing**

![Clock Diagram]

- Inverted clock is not ideal
- Causes delays on the clock
- Overlapping clock pair

**Register Design**

- Use non-overlapping clocks

**Register Parameters**

![Waveform Diagram]
Clock Non-idealities

- Clock Skew
  - Spatial variations in equivalent clock edges
  - Mostly deterministic
- Clock Jitter
  - Temporal variations in consecutive clock edges
  - Mostly random

Clock Uncertainties

- Clock Signal Generation
  - Analog circuit sensitive to noise
  - Causes jitter
  - Difficult to model
- Device Manufacturing
  - Process variations
  - Causes static skew
  - Can be partially modeled
- Interconnect variations
  - Causes skew on different paths
  - Different inter-layer dielectric thickness
  - Can be somewhat predictable based on process
- Temperature
  - Dependent on switching activity
  - Parts of a chip may see different temperatures
  - Contributes to clock jitter
- Power supply variations
  - Dependent on switching activity
  - Causes jitter
- Capacitive coupling
  - Between clock and adjacent lines
  - Transitions on adjacent lines can cause varying coupling effects
  - Net effect is jitter on the clock
- Skew and jitter can affect the cycle times
- Clock skew can cause race conditions
Positive and Negative Skew

Positive Skew

Launching edge arrives before the receiving edge

Negative Skew

Negative Skew

Receiving edge arrives before the launching edge

Clock Skew

Minimum cycle time:
\[ T + \delta \geq t_{c-q} + t_{su} + t_{logic} \]

Clock Jitter

Longest Logic Path in Edge-Triggered Systems

\[ t - t_{setup} \geq t_{c-q} + t_{logic} + t_{su} \]

Latest point of launching
Earliest arrival of next cycle
Setup problem
Shortest Path

Race-through problem

Clock Skew and Jitter

- Minimum clock cycle
  \[ T > t_{c-q} + t_{\text{logic}} + t_{\text{su}} - \delta + 2t_{jitter} \]

- Minimum logic delay
  \[ t_{\text{logic}} + t_{c-q} > t_{\text{hold}} + \delta + 2t_{jitter} \]

Clock Skew in systems with feedback

Clock Distribution

- Distribute clock in a tree fashion
- H-Tree

Clock Distribution

- Grid Structure

Clock Distribution

- Alpha 21064
  - 200 MHz clock, 5 levels of buffering
  - Clock load - 3.25nF
  - Clock drivers account for 40% of the switched capacitance
  - 200 ps maximum skew
- Alpha 21164
  - 300 MHz clock
  - Clock load - 3.75 nF
  - Clock distribution - 20W power dissipation - 40% of total power of processor
Clock Distribution

- Alpha 21164

Clock Distribution

- Pentium III
  - Clock Jitter - 10% of cycle
  - Clock Skew - 7% of cycle
- Pentium IV
  - Clock Jitter - 5% of cycle
  - Clock Skew - 3% of cycle
  - Used regional clock buffers with adjustable delay

Dealing with Clock Skew and Jitter

- Balance clock paths (Tree distribution)
- Shield clock signals to avoid coupling
  - Route clock next to VDD and GND
- Use dummy fills to have uniform interlayer dielectric thickness