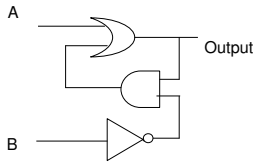
Topics

- Sequential Design
- Memory and Control

Sequential Logic

- In this course:
  - a latch is level sensitive
  - a register is edge-triggered
  - a flip-flop is bistable
- There are many different naming conventions
  - For instance, many books call edge-triggered registers flip-flops as well

Bistable Flip-Flop



Normally, A=0 B=0

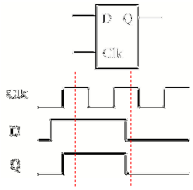
If A is set to 1, then Q=1. Q remains to be 1 even if A is set back to 0.

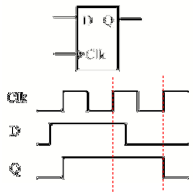
If B is set to 1, then Q=0. Q remains to be 0 even if B is set back to 0.

Use A to write 1 into this memory
Use B to write 0 into this memory

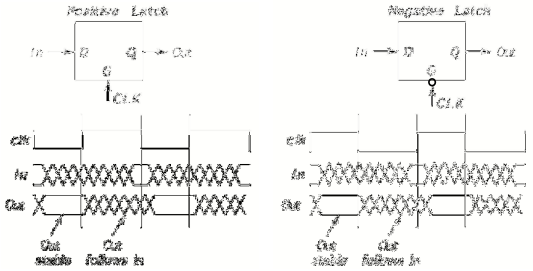
Latch versus Register

- Latch
  Stores data when clock is low
- Register
  Stores data when clock rises





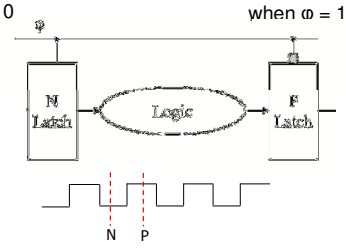
Latches



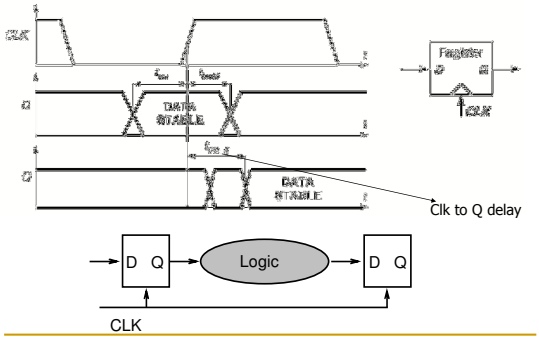
Commonly used in async. circuits

Latch-Based Design

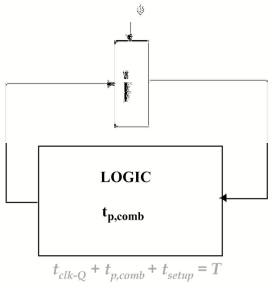
- N latch is transparent when φ = 0
- P latch is transparent when φ = 1



Timing Definitions



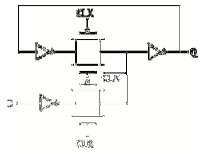
Maximum Clock Frequency



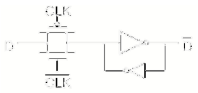
$$t_{clk\text{-}Q} + t_{p,comb} + t_{setup} = T$$

Writing into a Static Latch

- Use clock as a decoupling signal that distinguishes between the transparent and opaque states

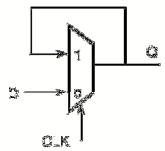


Converting into a MUX



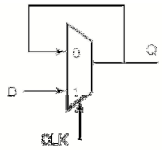
Forcing the state

Mux-Based Latches



$$Q = CLK \cdot Q + \overline{CLK} \cdot In$$

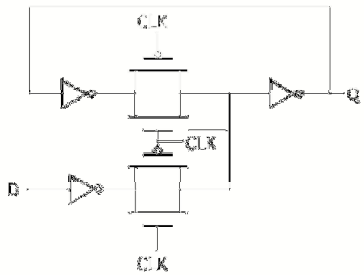
Negative latch
(transparent when CLK=0)



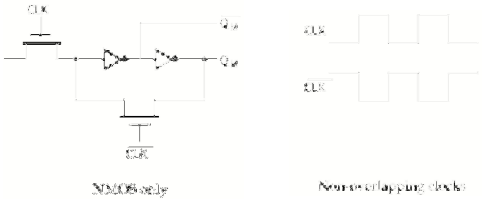
$$Q = \overline{CLK} \cdot Q + CLK \cdot In$$

Positive latch
(transparent when CLK=1)

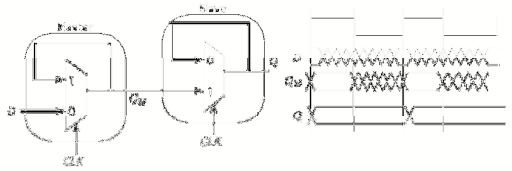
Mux-Based Latch



Mux-Based Latch



Master-Slave (Edge-Triggered) Register

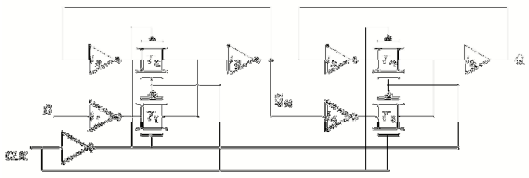


Two opposite latches

Also called master-slave latch pair

Master-Slave Register

Multiplexer-based latch pair

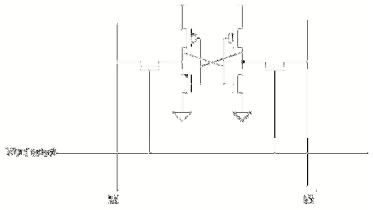


Semiconductor Memory Classification

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	Non-Random Access	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register		

Memory Design

- Static RAM Cell

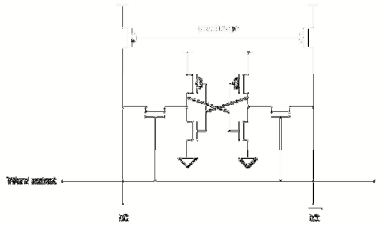


Memory Design

- Reads are straightforward
  - May need pre-charge circuitry to pull up bit line
- Writes are trickier
  - Use driver transistors that will pull-up or pull-down bit line as necessary

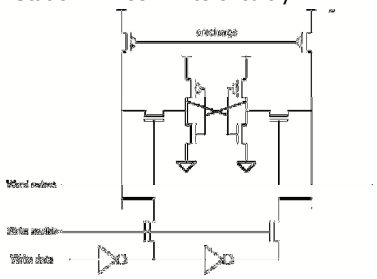
Memory Design

- Static RAM Cell with pre-charge

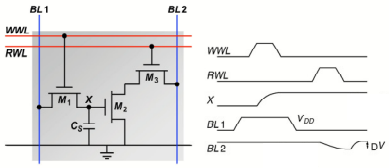


Memory Design

- Static RAM Cell write circuitry

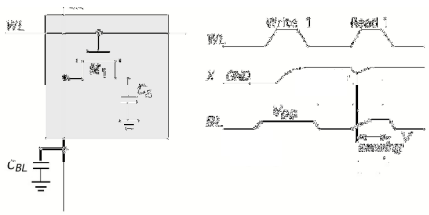


3-Transistor DRAM Cell



No constraints on device ratios
Reads are non-destructive
Value stored at node X when writing a "1" = V_{WWL}-V_{Tn}

1-Transistor DRAM Cell



Write: C_S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes places between bit line and storage capacitance

$$\Delta V = V_{BL} - V_{PRE} = V_{HIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design