Topics

- Sequential Design
- Memory and Control

Sequential Logic

- In this course:
  - a latch is level sensitive
  - a register is edge-triggered
  - a flip-flop is bistable
- There are many different naming conventions
  - For instance, many books call edge-triggered registers flip-flops as well

Bistable Flip-Flop

Normally, A=0 B=0
If A is set to 1, then Q=1. Q remains to be 1 even if A is set back to 0.
If B is set to 1, then Q=0. Q remains to be 0 even if B is set back to 0.
Use A to write 1 into this memory
Use B to write 0 into this memory

Latch versus Register

- Latch
  Stores data when clock is low
- Register
  Stores data when clock rises

Latches

- N latch is transparent when $\varphi = 0$
- P latch is transparent when $\varphi = 1$

Commonly used in async. circuits
Timing Definitions

- Clk to Q delay

Maximum Clock Frequency

- \[ f_{\text{clock}} = f_{\text{CO2}} + f_{\text{CO2}} + f_{\text{CO2}} + \ldots \]

Writing into a Static Latch

- Use clock as a decoupling signal that distinguishes between the transparent and opaque states

Mux-Based Latches

- Negative latch (transparent when CLK=0)
- Positive latch (transparent when CLK=1)

Mux-Based Latch

- Converting into a MUX
- Forcing the state
**Master-Slave (Edge-Triggered) Register**

Two opposite latches
Also called master-slave latch pair

**Master-Slave Register**

Multiplexer-based latch pair

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**Semiconductor Memory Classification**

<table>
<thead>
<tr>
<th>Read-Write Memory</th>
<th>Non-Volatile Read-Write Memory</th>
<th>Read-Only Memory</th>
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<tr>
<td>Random Access</td>
<td>Non-Random Access</td>
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<tr>
<td>SRAM</td>
<td>FIFO</td>
<td>EPROM</td>
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<tr>
<td>DRAM</td>
<td>LIFO</td>
<td>e²-PROM</td>
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<td></td>
<td></td>
<td>Mask-Programmed Programmable (PMOLAM)</td>
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**Memory Design**

- Reads are straightforward
  - May need pre-charge circuitry to pull up bit line
- Writes are trickier
  - Use driver transistors that will pull-up or pull-down bit line as necessary

**Memory Design**

- Static RAM Cell with pre-charge
Memory Design

- Static RAM Cell write circuitry

3-Transistor DRAM Cell

- No constraints on device ratios
- Reads are non-destructive
- Value stored at node X when writing a “1” = \( V_{\text{WWL}} - V_{\text{Tn}} \)

1-Transistor DRAM Cell

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design

DRAM Cell Observations