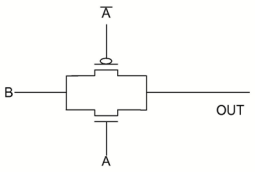
Topics

- Pass-transistor Logic
- Dynamic CMOS

Pass-Transistor Logic

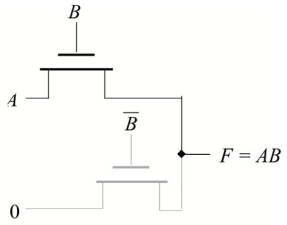
- Transmission Gate



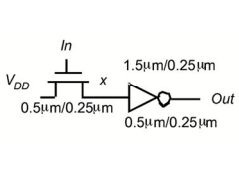
A	B	OUT
0	0	Z
0	1	Z
1	0	0
1	1	1

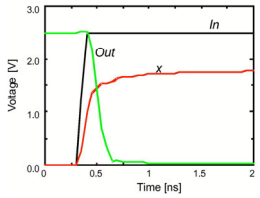
Pass-Transistor Logic

- Example: AND Gate

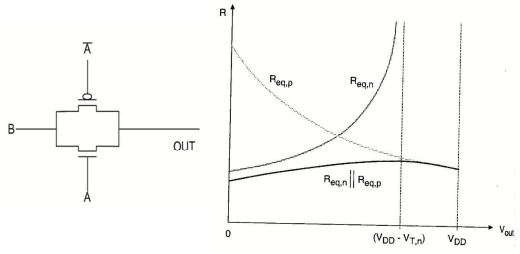


NMOS-Only Logic



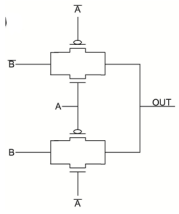


Resistance of Transmission Gate



Pass-Transistor Logic

- XOR



A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Pass-Transistor Logic

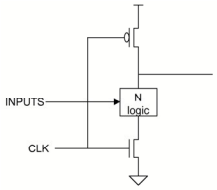
- In many cases, uses fewer transistors
- Can be difficult to design
- Usually requires complemented versions of all signals
- Difficult to layout
- Transmission gate looks like a RC line
- Delay analysis is not as well defined in terms of sizing choices

Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or VDD via a low resistance path.
  - fan-in of *n* requires 2*n* transistors (*n* N-type and *n* P-type)
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires only *n*+2 (*n*+1 N-type and 1 P-type) transistors (can be further reduced to *n*+1)

Dynamic CMOS

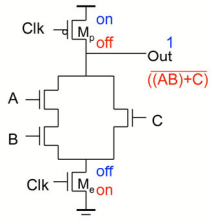
- nMOS logic structure with pre-charged pullup



•Pre-charge to VDD when clock is low

•Evaluate when clock is high

Dynamic Gate



Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next pre-charge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L

Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Sizing of the devices does not affect the logic levels (ratioless)

Properties of Dynamic Gates

- Faster switching speeds
  - reduced load capacitance due to smaller input capacitance (C_{in})
  - reduced load capacitance due to smaller output loading (C_{out})
  - Ideally, no I_{sc}, so all the current provided by PDN goes into discharging C_L

Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS (mainly due to clock)
  - no static current path exists between VDD and GND
  - no glitching (static CMOS has many glitches)
  - higher transition probabilities
  - extra load on Clk

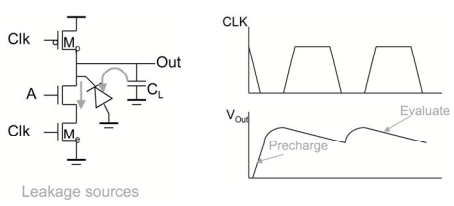
Properties of Dynamic Gates

- PDN starts to work as soon as the input signals exceed V_{Tn},
  - low noise margin (NML)
- Needs a pre-charge/evaluate clock

Dynamic CMOS

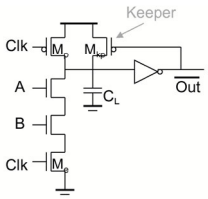
- Advantages
  - Fewer transistors than CMOS
  - Smaller load capacitance - faster speed
- Disadvantages
  - Leakage
  - Charge sharing
  - Cannot be cascaded directly
  - Only 0→1 transitions allowed at inputs, thus cannot be connected to static gate directly

Issues in Dynamic Design 1: Charge Leakage



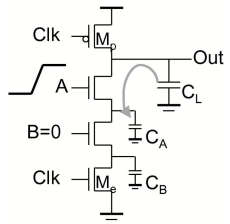
Dominant component is sub-threshold current

Solution to Charge Leakage



- Increase size of inverter to increase capacitance

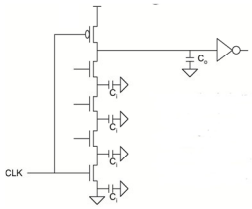
Issues in Dynamic Design 2: Charge Sharing



Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness

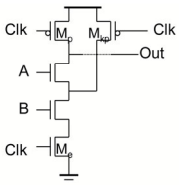
Dynamic CMOS

- Charge Sharing



- Assume that the internal capacitances have been discharged
- In the pre-charge phase, the output capacitance gets charged
- During evaluation, if all the inputs are high except the bottom one, the output capacitance gets distributed to the internal capacitance
- The output voltage will drop to $V_{DD}\frac{C_o}{C_o+2C_i}$
- This could be low enough to trigger the inverter, causing a wrong value on the output

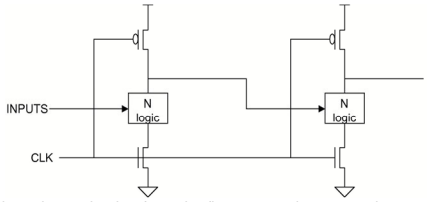
Solution to Charge Sharing



Pre-charge internal nodes using a clock driven transistor (at the cost of increased area and power)

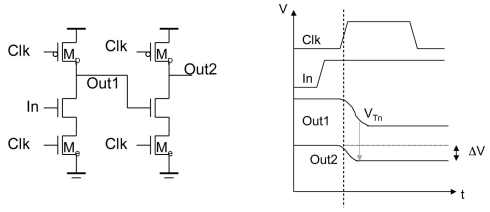
Dynamic CMOS

- Cascade problem



Since the evaluation from the first stage takes some time, the second stage will start evaluating with the pre-charged internal value rather than the inputs

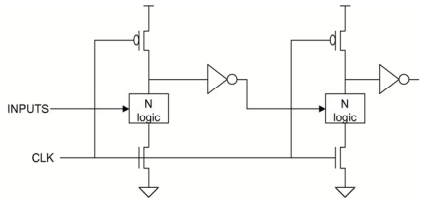
Cascading Dynamic Gates



Only 0 → 1 transitions allowed at inputs!

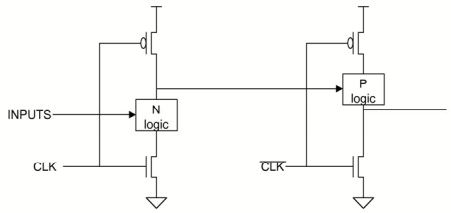
Domino Logic

- Solves cascade problem



Since the pre-charged output from the first stage is 0, it will never activate the pull-down network in the second stage until the first stage evaluation has completed.

NP Domino (Zipper) CMOS



Since the second stage is build from p-logic, the pre-charged output from the first stage will not activate the inputs of the second stage