Topics

- CMOS Logic Delays
- Logical Effort

Multi-input Delay

Input Pattern Effects on Delay

NAND

- Delay is dependent on the pattern of inputs (input combination)
- **Low to high transition**
  - both inputs go low
    - delay is $0.69 \frac{R_p}{2} C_L$
  - one input goes low
    - delay is $0.69 R_n C_L$
- **High to low transition**
  - both inputs go high
    - delay is $0.69 (2 R_n) C_L$

Delay Dependence on Input Patterns

Fan-In Considerations

4-input NAND gate

- Distributed RC model
  - Elmore delay
  - $t_{lep} = \frac{0.69}{R_{lep}} \left( C_1 + C_2 + 2 C_3 + 4 C_4 \right)$
- Propagation delay deteriorates rapidly as a function of fan-in in a quadratic manner in the worst case.

CMOS Logic Gate Delays

- Using **Logical Effort** to simplify delay calculation
- Helps in deciding
  - Transistor sizing
  - Number of stages
  - Circuit Topology
Characterize process speed with delay parameter $t_{pd}$
- $d = \frac{d_{abs}}{t_{pd}}$
- $t_{pd} \approx 20$ps for a .25 micron process

Process independent delay has two components
- $d = p + h$
- $h$ is the effort delay
- $p$ is the parasitic delay

Effort delay has two components
- $h = g*f$
- $g$ is the logical effort
- $f$ is the electrical effort or effective fanout

Parasitic delay is the delay due to intrinsic delay of gate - mostly the drain capacitance
- Independent of output load and sizing
- Approximately equal to 1 for an inverter

Logical effort is a measure of the gate’s ability to deliver current
- An inverter has a logical effort of 1
- Depends only on topology not on process or sizing

Electrical effort is a measure of fanout
- $C_{out}/C_{in}$

Logical Effort assignment
- Ratio of the gate’s input capacitance to the input capacitance of an inverter delivering the same amount of current
- Can be derived through simulations and accurate measurement
- Or through estimations based on transistor widths

Inverter

\[
\begin{array}{c}
A \quad 2x \\
\quad 1x \\
\hline
\hline
\end{array}
\]

$C_{in} = 3$
$g = \text{LogicalEffort} = 1$

NAND

\[
\begin{array}{c}
A \\
B \\
\hline
\hline
\end{array}
\]

$C_{in} = 4$
$g = \text{LogicalEffort} = 4/3$
Logical Effort

- NOR

\[ C_n = 5 \]
\[ g = \text{Logical Effort} = 5/3 \]

Logical Effort

- NOR

\[ C_n = 7 \]
\[ g = \text{Logical Effort} = 7/3 \]

Logical Effort

- Parasitic delay

<table>
<thead>
<tr>
<th>Number of inputs</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>n</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>2 ( p_{inv} )</td>
<td>3 ( p_{inv} )</td>
<td>( n ) ( p_{inv} )</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>2 ( p_{inv} )</td>
<td>3 ( p_{inv} )</td>
<td>( n ) ( p_{inv} )</td>
<td></td>
</tr>
</tbody>
</table>

Logical Effort

- Example: Inverter ring oscillator

- Estimate the frequency of the oscillator
Logical Effort

- Example: Inverter ring oscillator
  
  \[ g_i = 1 \]
  
  \[ f_i = 1 \]
  
  \[ p_i = 1 \]
  
  \[ d_i = g_i f_i + p_i = 2 \]

- Total delay = \( N \cdot d_i \cdot t_{p0} = 2N \cdot t_{p0} \)
  
  Frequency = \( 1/(4N \cdot t_{p0}) \)

Logical Effort

- Example: Fo4 Inverter (Fanout of 4)
  
  \[ g_i = 1 \]
  
  \[ f_i = 4 \]
  
  \[ p_i = 1 \]
  
  \[ d_i = g_i f_i + p_i = 5 \]

Logical Effort

- Multistage logic networks
  
  Path Parasitic Delay
  
  \[ P = \sum p_i \]

  Path Delay
  
  \[ D = P + \sum g_i f_i \]

  How do we minimize \( D \)? How do we select the sizing?

- Path effort is an indirect measure of the path delay
  
  - Path Electrical Effort
  
  - Path Logical Effort
  
  - Path Effort
    
  The above does not include any consideration of the effect of fanout within the path
  
  - \( H \) counts only the fanout of the output
  
  - We need to express the branching behavior along the path
Logical Effort

- Branching Effort

\[ b = \frac{C_{\text{on-path}} + C_{\text{off-path}}}{C_{\text{on-path}}} = \frac{C_{\text{out}}} {C_{\text{in}}} \]

\[ B = \prod b_i \]

\[ FB = \frac{C_{\text{in}}}{C_{\text{out}}} \times \prod b_i = \prod f_i \]

Logical Effort

- Path Effort

\[ H = G \times FB = \prod b_i \cdot \prod f_i = G \cdot F \]

- Path Delay

\[ D = P + \sum b_i \cdot \sum f_i \]

- Minimized when each stage delay is equal

\[ G \cdot F = k = \sqrt{H} \]

\[ D = P + N \cdot \sqrt{H} \]

Logical Effort

- Example

\[ G = \prod e = 1 \times 2 \times 2 = 4 \]

\[ h = \frac{20}{10} = 2 \]

\[ B = 1 \]

\[ H = G \times FB = \frac{100}{27} \times 1 = \frac{100}{27} \]

Logical Effort

- Example

\[ G = \prod e = 1 \times 2 \times 2 = 4 \]

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\[ H = G \times FB = \frac{100}{27} \times 1 = \frac{100}{27} \]
Logical Effort

- Example (cont)

\[
\begin{align*}
\hat{k} &= \frac{C}{V} = \frac{10}{1} = 10 \\
\hat{k} &= g_J \frac{4}{3} = \frac{4}{3} \times 10 = 5.16 = \Rightarrow z = 2.58
\end{align*}
\]