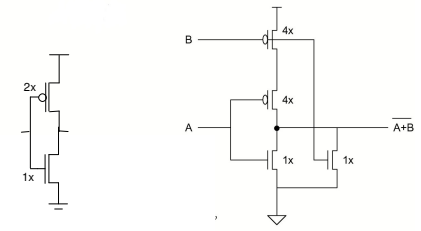
Topics

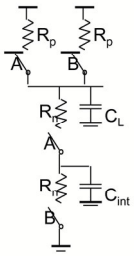
- CMOS Logic Delays
- Logical Effort

Multi-input Delay



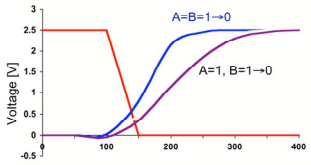
Input Pattern Effects on Delay

NAND



- Delay is dependent on the pattern of inputs (input combination)
- **Low to high transition**
  - both inputs go low
    - delay is 0.69 (R_p/2) C_L
  - one input goes low
    - delay is 0.69 R_p C_L
- **High to low transition**
  - both inputs go high
    - delay is 0.69 (2 R_n) C_L

Delay Dependence on Input Patterns

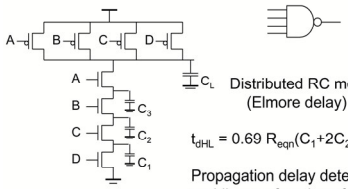


Input Data Pattern	Delay (psec)
00→11	69
10→11	62
01→11	50
11→00	35
11→10	76
11→01	57

NMOS = 0.5μm/0.25 μm
PMOS = 0.75μm/0.25 μm
C_L = 100 fF

Fan-In Considerations

4-input NAND gate



Distributed RC model (Elmore delay)

$t_{dHL} = 0.69\ R_{eqn}(C_1+2C_2+3C_3+4C_L)$

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.

• Gates with a fan-in greater than 4 should be avoided

CMOS Logic Gate Delays

- Using Logical Effort to simplify delay calculation
- Helps in deciding
  - Transistor sizing
  - Number of stages
  - Circuit Topology

Logical Effort

- Characterize process speed with delay parameter t_{p0}
  - $d = d_{abs}/ t_{p0}$
  - $t_{p0} \approx 20ps$ for a .25 micron process
- Process independent delay has two components
  - d=p+h
  - h is the effort delay
  - p is the parasitic delay

Logical Effort

- Effort delay has two components
  - h=g*f
  - g is the logical effort
  - f is the electrical effort or effective fanout
- Parasitic delay is the delay due to intrinsic delay of gate - mostly the drain capacitance
  - Independent of output load and sizing
  - Approximately equal to 1 for an inverter

Logical Effort

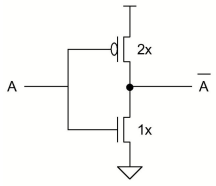
- Logical effort is a measure of the gate's ability to deliver current
  - An inverter has a logical effort of 1
  - Depends only on topology not on process or sizing
- Electrical effort is a measure of fanout
  - C_{out}/C_{in}

Logical Effort

- Logical Effort assignment
  - Ratio of the gate's input capacitance to the input capacitance of an inverter delivering the same amount of current
  - Can be derived through simulations and accurate measurement
  - Or through estimations based on transistor widths

Logical Effort

- Inverter

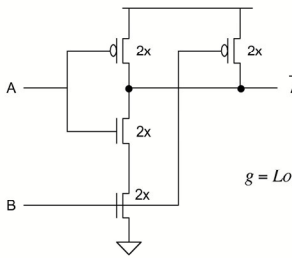


$C_{in} = 3$

$g = LogicalEffort = 1$

Logical Effort

- NAND

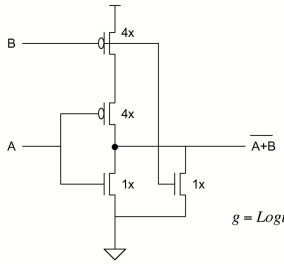


$C_{in} = 4$

$g = LogicalEffort = 4/3$

Logical Effort

- NOR

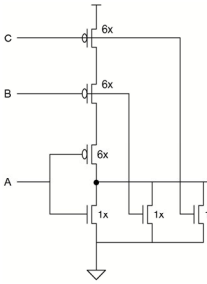


$C_{in} = 5$

$g = LogicalEffort = 5/3$

Logical Effort

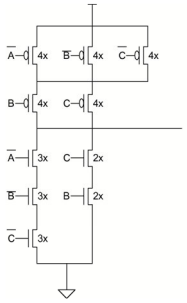
- NOR



$C_{in} = 7$

$g = LogicalEffort = 7/3$

Logical Effort



$C_{inA} = 7$

$g_{\bar{A}} = LogicalEffort = 7/3$

Logical Effort

Number of inputs	1	2	3	n
INV	1			
NAND		4/3	5/3	(n+2)/3
NOR		5/3	7/3	(2n+1)/3

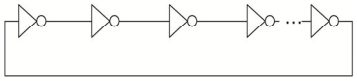
Logical Effort

- Parasitic delay

Number of inputs	1	2	3	n
INV	p_{inv}			
NAND		$2\ p_{inv}$	$3\ p_{inv}$	$n\ p_{inv}$
NOR		$2\ p_{inv}$	$3\ p_{inv}$	$n\ p_{inv}$

Logical Effort

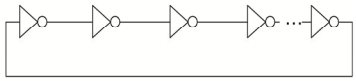
- Example: Inverter ring oscillator



- Estimate the frequency of the oscillator

Logical Effort

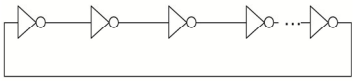
- Example: Inverter ring oscillator



- $g_i = 1$
- $f_i = 1$
- $p_i = 1$
- $d_i = g_i f_i + p_i = 2$

Logical Effort

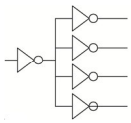
- Example: Inverter ring oscillator



- Total delay = $N \bullet d_i \bullet t_{p0} = 2N\, t_{p0}$
- Frequency $= 1/(4N\, t_{p0})$

Logical Effort

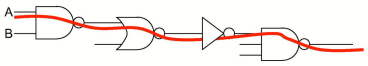
- Example: FO4 Inverter (Fanout of 4)



- $g_i = 1$
- $f_i = 4$
- $p_i = 1$
- $d_i = g_i f_i + p_i = 5$

Logical Effort

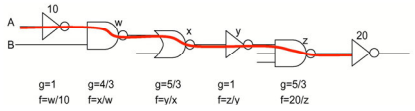
- Multistage logic networks



- Find path delay

Logical Effort

- Multistage logic networks



- Path Parasitic Delay

$$P = \sum p_i$$

- Path Delay

$$D = P + \sum g_i f_i$$

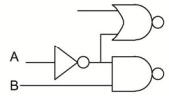
- How do we minimize D? How do we select the sizing?

Logical Effort

- Path effort is an indirect measure of the path delay
  - Path Electrical Effort $F = \frac{C_{out}}{C_{in}}$
  - Path Logical Effort $G = \prod g_i$
  - Path Effort $H = GF$
- The above does not include any consideration of the effect of fanout within the path
  - H counts only the fanout of the output
  - We need to express the branching behavior along the path

Logical Effort

- Branching Effort



$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}} = \frac{C_{total}}{C_{useful}}$$

$$B = \prod b_i$$

$$FB = \frac{C_{out}}{C_{in}} \prod b_i = \prod f_i$$

Logical Effort

- Path Effort

$$H = G \times FB = \prod g_i \prod f_i = \prod g_i f_i$$

- Path Delay

$$D = P + \sum g_i f_i$$

- Minimized when each stage delay is equal

$$g_i f_i = \hat{h} = \sqrt[N]{H}$$

$$D = P + N\hat{h}$$
$$= P + N\sqrt[N]{H}$$

Logical Effort

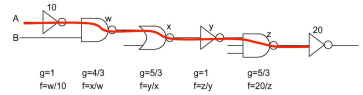
- Work backwards to assign sizing

$$g_i f_i = \sqrt[N]{H}$$

$$f_i = \frac{\sqrt[N]{H}}{g_i}$$

Logical Effort

- Example



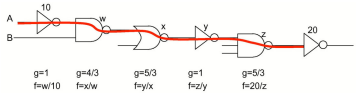
$$G = \prod g_i = 1 \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot 1 \cdot \frac{5}{3} = \frac{100}{27}$$

$$F = \frac{C_{out}}{C_{in}} = \frac{20}{10} = 2$$

$$B = 1$$

$$H = G \times FB = \frac{100}{27} \cdot 2 \cdot 1 = \frac{200}{27}$$

Logical Effort



$$\hat{h} = \sqrt[N]{H} = \sqrt[3]{\frac{200}{27}} = 1.49$$

$$\hat{h} = g_5 f_5 = \frac{5}{3} \cdot \frac{20}{z} = 1.49 \Rightarrow z = 22.3$$

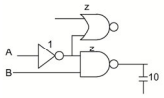
$$\hat{h} = g_4 f_4 = 1 \cdot \frac{z}{y} = 1.49 \Rightarrow y = 15.0$$

$$\hat{h} = g_3 f_3 = \frac{5}{3} \cdot \frac{y}{x} = 1.49 \Rightarrow x = 16.8$$

$$\hat{h} = g_2 f_2 = \frac{4}{3} \cdot \frac{x}{w} = 1.49 \Rightarrow w = 15.0$$

Logical Effort

- Example



$$G = \prod g_i = 1 \cdot \frac{4}{3} = \frac{4}{3}$$

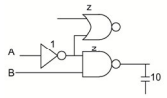
$$F = \frac{C_{out}}{C_{in}} = \frac{10}{1} = 10$$

$$B = \frac{C_{total}}{C_{onpath}} = \frac{2z}{z} = 2$$

$$H = G \times FB = \frac{4}{3} \cdot 10 \cdot 2 = \frac{80}{3}$$

Logical Effort

- Example (cont)



$$\hat{h} = \sqrt[N]{H} = \sqrt[1]{\frac{80}{3}} = 5.16$$

$$\hat{h} = g_2 f_2 = \frac{4}{3} \cdot \frac{10}{z} = 5.16 \Rightarrow z = 2.58$$