Design rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter

Layout Styles

- Vertical transistors

Layout Styles

- Horizontal transistors

Wiring Tracks

- A wiring track is the space required for a wire
  - 4 lambda width, 4 lambda spacing from neighbor = 8 lambda pitch

Well Spacing

- Wells must surround transistors by 6 lambda
  - Implies 12 lambda between opposite transistor flavors
  - Leaves room for one wire track

Shared Diffusion Area

- A - B
Example: NAND Gate

Area Estimation

- Estimate area by counting wiring tracks

Layout Strategies

- How do you decide on a layout?
  - Area constraints
  - Requirements of inputs and outputs
  - Metal layer interconnect
  - Difficult for multi-input gates
    - How do you decide on order of inputs?

Layout Strategies

- Euler path method
- Convert schematic into a graph
- Eg. \[ F = AB + C + DE \]

Layout Strategies

- Find common path in both graphs (Euler path)
  - A to B to C to D to E
Layout Strategies

- Euler path method
  - Not always guaranteed to find a Euler path
  - For example, if the function was
    \[ F = C \land AB \lor DE \]
  - If no Euler path found, you will need to break the gate, or rearrange the inputs

- Very wide transistors
  - Multiple contacts to reduce diffusion resistance
  - Folding to reduce diffusion capacitance

- Performance implications
  - Number of transistors at output
  - Order of transistors
• Ordering of inputs
  - If A arrives before B, it will charge up the capacitance to VDD. When B arrives, it needs to discharge the capacitor.
  - If B arrives before A, the capacitor will be discharged before A arrives.
  - Try and put the early arriving signal close to ground - can speed NAND up to 20%
Layout Choices

- Interconnect
  - Keep VDD and VSS in the highest level metal
  - Within a single cell, use a single layer of metal so you can route other metal layers above the cell
  - Don’t have long runs of poly

Layout Choices

- Consider how low level cells will interconnect with each other
- Minimize locally and compact globally
- Find critical areas first and then optimize

Layout Process

- Layout vs. Schematic (LVS)
  - Make sure that the layout matches your schematic
- Design Rule Check (DRC)
  - Check if all design rules are met