## Delay time analysis

- As with interconnect delay, find the equivalent resistance and load capacitance of the transistor

$$t_{pHL} = .69 R_{eqn} C_L$$

- Take average of p and n delays for overall propagation delay

$$t_p = .69 C_L \left( \frac{R_{eqn} + R_{eqp}}{2} \right)$$



## Delay time analysis

- The delay time is affected by the load capacitance and the transistor *K*'s
- Reduce delay by
  - Reducing $C_L$
  - Increasing *k*
  - Increasing *W/L* ratio
  - Increasing $V_{DD}$



## Delay time analysis

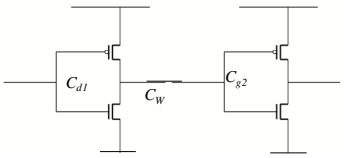
- In order to equalize the rise and fall delays, the transistor equivalent resistances must be equal
- Typically that means the pMOS width must be 2-3 times the width of the nMOS to have equal falling and rising delay times
- However, this does not mean that overall delay has been minimized



## Delay time analysis

- Assume that the inverter is cascaded to another inverter

$$t_p = 0.69 R_{eq} \left( (C_{dp1} + C_{dn1}) + (C_{gp2} + C_{gn2}) + C_W \right)$$






## Delay time analysis

- Scale the pMOS transistors by a factor of β

$$t_p = 0.69 \left( \frac{R_{eqn} + R_{eqp}/\beta}{2} \right) \left( (\beta C_{dp1} + C_{dn1}) + (\beta C_{gp2} + C_{gn2}) + C_W \right)$$

$$= 0.345 \left( R_{eqn} + \frac{R_{eqp}}{\beta} \right) \left( (\beta + 1)(C_{dn1} + C_{gn2}) + C_W \right)$$

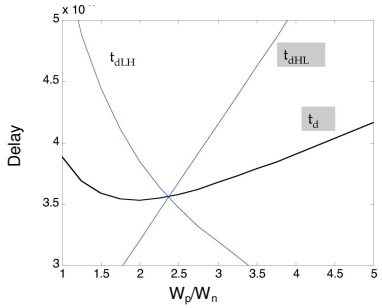
$C_{dp1} = C_{dn1}$
$C_{gp2} = C_{gn2}$

- Optimal β

$$\beta = \sqrt{\frac{R_{eqp}}{R_{eqn}}} \approx \sqrt{\frac{k_n V_{DSATn}}{k_p V_{DSATp}}}$$

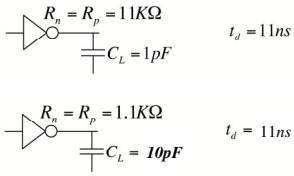


## PMOS/NMOS ratio



## Transistor Sizing

- Size the transistors based on delay requirements and capacitor load





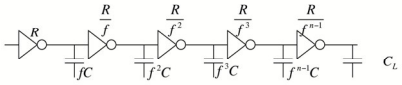

## Transistor Sizing

- Increasing transistor size allows us to drive large capacitances
- Problems
  - Increases area
  - Increases input capacitance



## Transistor Sizing

- Use cascaded inverters




$$t_f = (n-1)fRC + \frac{R}{f^{n-1}}C_L$$

If we equalize the delays, then $f^n = \frac{C_L}{C}$

$$t_p = nfRC$$



## Transistor Sizing

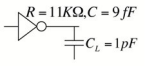
$$t_p = nfRC$$

$$f^n = \frac{C_L}{C} \quad \Rightarrow \quad = \frac{\ln\left(\frac{C_L}{C}\right)}{\ln f} fRC$$

- Minimum delay is reached when $f$ is equal to $e$ (~2.72)
- At optimum, $n = \ln\left(\frac{C_L}{C}\right)$



## Transistor Sizing




$$n = \ln\left(\frac{C_L}{C}\right) = \ln\left(\frac{1pF}{9fF}\right) = 4.71$$

Set $n$=5, and $f$ =3 to use integral values

$$t_f = (n-1)fRC + \frac{R}{f^{n-1}}C_L$$
$$= (5-1)\cdot 3 \cdot 11K\Omega \cdot 9fF + \frac{11K\Omega}{3^{5-1}}1pF$$
$$= 1.32ns$$



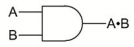
## Transistor Sizing

- Cascaded inverter staging will use more area than a single inverter
- The input capacitance is much lower
- The number of stages and stage ratio can be adjusted to get faster delay times or smaller area
- When you take into account intrinsic capacitance, the optimal $f$ will be different than $e$

## Boolean Algebra

- Basic operators
  - AND

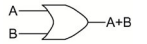
$f(A,B) = A \cdot B = A \cap B$




| A | B | A•B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

  - OR

$f(A,B) = A + B = A \cup B$




| A | B | A+B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



## Boolean Algebra

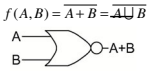
- Basic operators
  - NAND

$f(A,B) = \overline{A \cdot B} = \overline{A \cap B}$


| A | B | $\overline{A \cdot B}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

  - NOR

$f(A,B) = \overline{A + B} = \overline{A \cup B}$



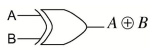

| A | B | $\overline{A+B}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |



## Boolean Algebra

- Basic operators
  - XOR

$f(A,B) = A \oplus B$




| A | B | $A \oplus B$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

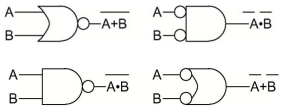


## Boolean Algebra

- DeMorgan's Theorem

$\overline{A + B} = \overline{A} \cdot \overline{B}$

$\overline{A \cdot B} = \overline{A} + \overline{B}$






## Boolean Algebra

- Truth Tables

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

  - Representation of the function to be realized
  - Sum of Products representation
    - Sum of minterms

$F = \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\overline{C} + A\overline{B}C + AB\overline{C}$

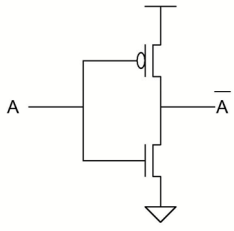
  - Product of Sums representation
    - Product of maxterms

$F = (A + B + C) \cdot (A + \overline{B} + \overline{C}) \cdot (\overline{A} + \overline{B} + \overline{C})$



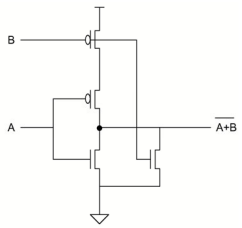
## CMOS Logic Implementations

- Inverter



## CMOS Logic Implementations

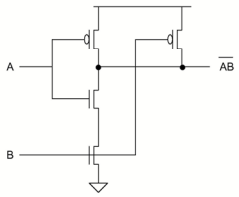
- NOR






## CMOS Logic Implementations

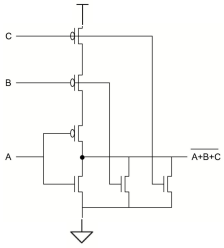
- NAND






## CMOS Logic Implementations

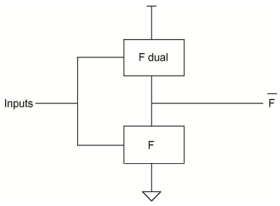
- Multi-input NOR






## CMOS Logic Implementations

- General CMOS combinational logic



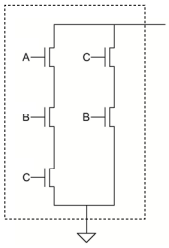



## CMOS Logic Implementations

$F = \overline{ABC + BC}$

$\overline{F} = ABC + BC$

Pulldown



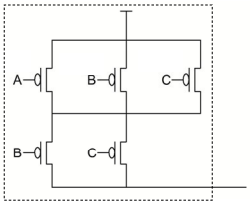



## CMOS Logic Implementations

$F = \overline{ABC + BC}$

$\overline{F} = ABC + BC$

Pullup



## CMOS Logic Implementations