Interconnect delay

- Lumped RC model

- Charge $V_n$ to $V_{DD}$
- The transient output voltage is

$$ V_{out}(t) = V_{DD} \left(1 - e^{-\frac{t}{RC}}\right) $$

$$ \tau_{DL} = \frac{1}{2} $$

$$ \tau_{DL} = 69RC $$

Elmore Delay

- Single line model not useful for generalized RC tree networks

RC-tree property:
- Unique resistive path between the source node $s$ and any other node $i$ of the network $\rightarrow$ path resistance $R_{ik}$

Example: $R_{54} = R_1 + R_3 + R_4$

Assuming:
- Each node is initially discharged to ground
- A step input (pulse) is applied at time $t=0$ at node $s$
- The Elmore delay at node $i$ is:

$$ \tau_{EL} = \sum_{k=1}^{N} C_i R_k $$

- It is an approximation: it is equivalent to first-order time constant of the network
- Proven acceptable
- Powerful mechanism for a quick estimate
Elmore Delay

- Examples

\[ \tau_1 = R(C_1) + (R + R_1)C_2 + (R + R_1 + R_1)C_3 + R_1C_4 \]

\[ \tau_2 = R(C_1) + R_1C_2 + R_1C_3 + (R + R_1)C_4 \]

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Interconnect Delay

- Fanout Effects
  - Lines with multiple loads will have longer delays
    - Clocks
    - Data buses
    - Control lines
  - Solutions
    - Wider lines for special signals
    - Buffers

\[ \tau = \frac{RC}{N+1} \left( \frac{N+1}{2} \right) \]

- Delay is proportional to the square of the length
- Try to avoid long lines

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Interconnect Delay

- Avoid long interconnect delays using buffers
  - Interconnect resistance
    - 5000\( \mu \)Ω (5.0 wide)
  - Interconnect capacitance
    - 5000\( \mu \)F (5.0 wide)
  - Intrinsic load capacitance
    - 5.0\( \mu \)F
  - Propagation delay
    - 184 ps

\[ \tau = \frac{RC}{2} + \frac{RC}{2} \left( \frac{200 \cdot 51.5 \cdot 5.0}{2} \right) = 184 \text{ ps} \]
Interconnect Delay

- Avoid long interconnect delays using wider lines
- Interconnect resistance
  \[ R = \frac{\mu \Omega}{1000 \text{ mil}} \]
- Interconnect capacitance
  \[ C_{\text{inter}} = \frac{5000 \mu \text{F} + 0.044 \cdot (5000 \mu \text{F} + 5\mu \text{F})}{1190} \]
- Intrinsic load capacitance
  \[ C_{\text{load}} = 5\mu \text{F} \]
- Propagation delay
  \[ t_p = \frac{RC_{\text{inter}}}{2} + \frac{RC_{\text{load}}}{2} = \frac{70}{2} \cdot 1190 \mu \text{F} + 70 \cdot 5 \mu \text{F} = 42 \mu \text{s} \]

Switching Delay

- The intrinsic delay of a gate
- Transistor sizing can affect the delay
- Extrinsic capacitances can affect the delay

Delay Definitions

Switching Delay

- Fall time analysis

Fall time analysis

- Saturation Mode
  \[ t_f = \frac{L_f}{I_f} \]
  \[ \frac{\partial V}{\partial t} = \frac{1}{2} \left( V_{\text{sat}} - V_{\text{in}} \right)^2 \]
  \[ dt = \frac{C_1}{C_2 (V_{\text{in}} - V_{\text{out}})} \]
  \[ t_f = \frac{C_1}{C_2 (V_{\text{out}} - V_{\text{in}})} \int_{V_{\text{in}}}^{V_{\text{sat}}} \left( \frac{\partial V}{\partial t} \right) \]

- Linear Mode
  \[ t_f = \frac{L_f}{I_f} \]
  \[ \frac{\partial V}{\partial t} = k \left( V_{\text{in}} - V_{\text{out}} \right)^2 \]
  \[ dt = \frac{2C_1}{k (V_{\text{in}} - V_{\text{out}})^2} \]
  \[ t_f = \frac{2C_1}{k (V_{\text{in}} - V_{\text{out}})^2} \int_{V_{\text{in}}}^{V_{\text{out}}} \left( \frac{\partial V}{\partial t} \right) \]
Fall time analysis

- Linear Mode

\[ t_f = \frac{C_{\text{fb}}}{k_n(V_{\text{DD}}-V_T)} \ln\left(\frac{V_{\text{DD}}-V_{out}}{V_{out}}\right) - \frac{C_{\text{fb}}}{k_n(V_{\text{DD}}-V_T)} \ln(V_{\text{DD}}-V_{out}) \]

Fall time analysis

- Fall time is proportional to load capacitance and inversely proportional to \( V_{\text{DD}} \) and \( k_n \)
- Decreasing the supply voltage will increase the fall time
- Increasing the transistor width will increase \( k_n \) which will reduce the fall time
- Changing these three parameters can cause conflicting goals

Rise time analysis

- For equal fall times and rise times

\[ t_f = t_r \]

\[ K_r = \frac{C_{\text{fb}}}{k_n(V_{\text{DD}}-V_T)} \left(\frac{2p-1}{1-p}\right) + \ln(V_{\text{DD}}-V_{out}) - \frac{1}{1-p} \ln(V_{\text{DD}}-V_{out}) \]

Propagation Delay

- As with interconnect delay, find the equivalent resistance and load capacitance of the transistor

\[ t_{\text{prop}} = 69R_sC_L \]
Propagation Delay

Where:

- $R_n = \text{avg}(R_i(t)) = \frac{1}{\text{i}_{-\infty}^{\infty} V_i(t) \, T_{\text{on}}(t)}$

- Propagation delay is the time for voltage to reach half way point - so integrate from $V_{\text{DD}}$ to $V_{\text{DD}}/2$

- For the output range we are interested in, the transistor is always in saturation

\[ R_n = \frac{2}{V_{\text{DD}}/2 - V_{\text{DD}}} \left( \int V_i(t) \, T_{\text{on}}(t) \right) \]

- Load capacitance

- Intrinsic capacitance - sum of capacitances at drain - $C_{GDO}$

- Extrinsic capacitance is composed of wire capacitance and input capacitance of fanout

- Input capacitance is composed of overlap capacitance and channel capacitance

- Overlap capacitance is $C_{GDO} + C_{GSO}$ (very small)

- Channel capacitance is $C_{oX}W_L$. Assume worst case

\[ I_{\text{sat}} = 0.69 R_e (2C_{\text{channel}} + 2C_{\text{device}} + C_{\text{in}} + C_{\text{ex}} + C_{\text{in}}) \]
Propagation Delay

- All capacitances are roughly proportional to \( W \)
- Equivalent resistance is inversely proportional to \( W \)