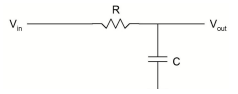
Interconnect delay

- Lumped RC model



- Charge V_{in} to V_{DD}
- The transient output voltage is

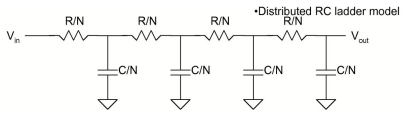
$$V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$$

$$\frac{V_{DD}}{2} = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$$

$$\frac{t_{dlh}}{RC} = -\ln\left(\frac{1}{2}\right)$$

$$t_{dlh} \approx .69RC$$

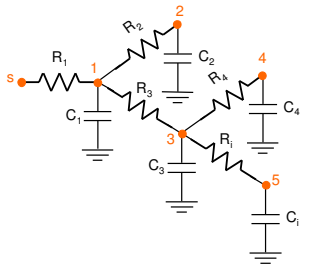
Interconnect delay



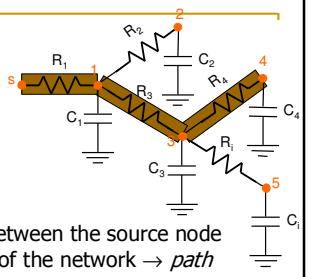
- More accurate than lumped RC model
- More difficult to solve for large N
- Need full-scale SPICE simulation

Elmore Delay

- Single line model not useful for generalized RC tree networks



Elmore Delay

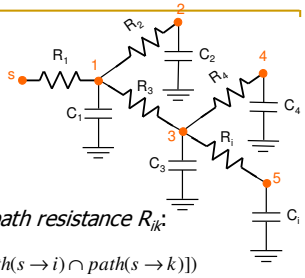


RC-tree property:

- Unique resistive path between the source node *s* and any other node *i* of the network → *path resistance* R_{ii}

  Example: $R_{44}=R_1+R_3+R_4$

Elmore Delay



RC-tree property:

- Extended to *shared path resistance* R_{ik}:

$$R_{ik} = \sum R_j \quad \text{s.t.} \quad (R_j \in [path(s \to i) \cap path(s \to k)])$$

Example: $R_{54}=R_1+R_3$

$R_{52}=R_1$

Elmore Delay

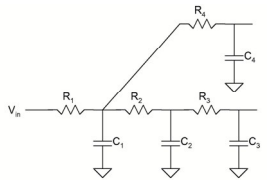
- Assuming:
  - Each node is initially discharged to ground
  - A step input (pulse) is applied at time *t=0* at node *s*
- The Elmore delay at node *i* is:

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

- It is an approximation: it is equivalent to first-order time constant of the network
  - Proven acceptable
  - Powerful mechanism for a quick estimate

Elmore Delay

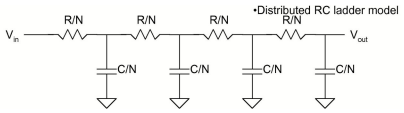
- Examples



$$t_{d3} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + R_1C_4$$

$$t_{d4} = R_1C_1 + R_1C_2 + R_1C_3 + (R_1 + R_4)C_4$$

Elmore Delay



$$t_d = \sum_{j=1}^{N} \frac{C}{N} \sum_{k=1}^{j} \frac{R}{N}$$

$$= \frac{C}{N}\frac{R}{N}\frac{N(N+1)}{2} = RC\left(\frac{N+1}{2N}\right)$$

$$t_d = \frac{RC}{2} \; for \; N \to \infty$$

Interconnect Delay

- **Fanout Effects**
  - Lines with multiple loads will have longer delays
    - Clocks
    - Data buses
    - Control lines
  - Solutions
    - Wider lines for special signals
    - Buffers

Interconnect Delay

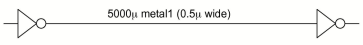
$$t_d = \frac{RC}{2}$$

$$= \tfrac{1}{2}\left(r\tfrac{l}{w}\right)(c_a lw + 2c_p(l+w))$$

$$\approx \tfrac{1}{2} rc_a l^2$$

- Delay is proportional to the square of the length
- Try to avoid long lines

Interconnect Delay



- Interconnect resistance

$$r.l/w \longrightarrow R = .07\frac{5000\mu}{0.5\mu} = 700\Omega$$

- Interconnect capacitance

$$C_a lw + 2C_p(l+w) \longrightarrow C_{wire} = .03 \cdot 5000\mu \cdot 0.5\mu + .044 \cdot 2 \cdot (5000\mu + 0.5\mu) = 515\,fF$$

- Intrinsic load capacitance

$$C_{in} \approx 5\,fF$$

- Propagation delay

$$t_p = \frac{RC_{wire}}{2} + RC_{in} = \left(\frac{700 \cdot 515\,fF}{2} + 700 \cdot 5\,fF\right) = 184\,ps$$

Interconnect Delay

- Avoid long interconnect delays using buffers

- Interconnect resistance

$$R = .07\frac{2500\mu}{0.5\mu} = 350\Omega$$

- Interconnect capacitance

$$C_{wire} = .03 \cdot 2500\mu \cdot 0.5\mu + .044 \cdot 2 \cdot (2500\mu + 0.5\mu) = 258\,fF$$

- Intrinsic load capacitance

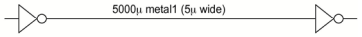
$$C_{in} \approx 5\,fF$$

- Propagation delay

$$t_p = \frac{RC_{wire}}{2} + RC_{in} = 2 \cdot \left(\frac{350 \cdot 258\,fF}{2} + 350 \cdot 5\,fF\right) = 94\,ps$$

Interconnect Delay

- Avoid long interconnect delays using wider lines



- Interconnect resistance

$$R = .07\frac{5000\mu}{5\mu} = 70\Omega$$

- Interconnect capacitance

$$C_{wire} = .03 \cdot 5000\mu \cdot 5\mu + .044 \cdot 2 \cdot (5000\mu + 5\mu) = 1190\,fF$$

- Intrinsic load capacitance

$$C_{in} \approx 5\,fF$$

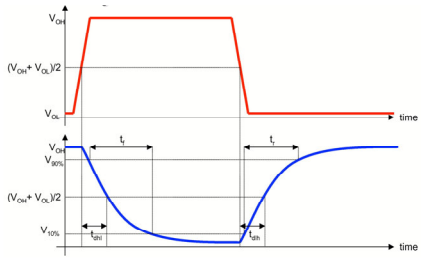
- Propagation delay

$$t_p = \frac{RC_{wire}}{2} + RC_{in} = \left(\frac{70 \cdot 1190\,fF}{2} + 70 \cdot 5\,fF\right) = 42\,ps$$

Switching Delay

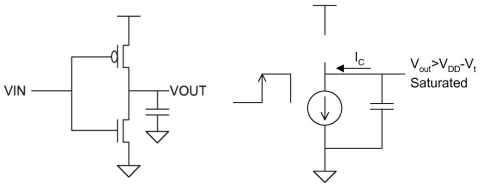
- The intrinsic delay of a gate
- Transistor sizing can affect the delay
- Extrinsic capacitances can affect the delay

Delay Definitions



Switching Delay

- **Fall time analysis**



Fall time analysis

- **Saturation Mode**

$$I_C = I_{DS}$$

$$-C_L\frac{dV_{out}}{dt} = k_n\frac{(V_{DD}-V_{tn})^2}{2}$$

$$dt = -2\frac{C_L}{k_n(V_{DD}-V_{tn})^2}dV_{out}$$

$$t_{f1} = 2\frac{C_L}{k_n(V_{DD}-V_{tn})^2}\int_{.9V_{DD}}^{V_{DD}-V_{tn}} dV_{out}$$

$$t_{f1} = 2\frac{C_L(V_{tn}-.1V_{DD})}{k_n(V_{DD}-V_{tn})^2}$$

Fall time analysis

- **Linear Mode**

$$I_C = I_{DS}$$

$$-C_L\frac{dV_{out}}{dt} = k_n\left[(V_{DD}-V_{tn})V_{out} - \frac{V_{out}^2}{2}\right]$$

$$dt = \frac{-2C_L}{k_n(2(V_{DD}-V_{tn})V_{out} - V_{out}^2)}dV_{out}$$

$$t_{f2} = \frac{-2C_L}{k_n}\int_{.1V_{DD}}^{V_{DD}-V_{tn}} \frac{dV_{out}}{(2V_{out}(V_{DD}-V_{tn}) - V_{out}^2)}$$

Fall time analysis

- **Linear Mode**

$$t_{f2} = \frac{C_L}{k_n(V_{DD} - V_m)} \ln\left(\frac{V_{out}}{2(V_{DD} - V_m) - V_{out}}\right)\Bigg|_{1V_{DD}}^{V_{DD}-V_m}$$

$$= \frac{C_L}{k_n(V_{DD} - V_m)} \ln\left(\frac{19V_{DD} - 20V_m}{V_{DD}}\right)$$

Fall time analysis

$$t_f = t_{f1} + t_{f2}$$

$$= \frac{C_L}{k_n(V_{DD} - V_m)}\left(\frac{2(V_m - .1V_{DD})}{V_{DD} - V_m} + \ln\left(\frac{19V_{DD} - 20V_m}{V_{DD}}\right)\right)$$

$$= \frac{C_L}{k_n(V_{DD} - V_m)}\left(\frac{2(n - .1)}{1 - n} + \ln(19 - 20n)\right) \qquad n = \frac{V_m}{V_{DD}}$$

$$K = \frac{1}{(1-n)}\left(\frac{2(n - .1)}{1 - n} + \ln(19 - 20n)\right)$$

$$t_f = K\frac{C_L}{k_n V_{DD}}$$

Fall time analysis

- Fall time is proportional to load capacitance and inversely proportional to V_{DD} and k_n
- Decreasing the supply voltage will increase the fall time
- Increasing the transistor width will increase k_n which will reduce the fall time
- Changing these three parameters can cause conflicting goals

Rise time analysis

$$t_r = \frac{C_L}{k_p V_{DD}(1-p)}\left(\frac{2(p - .1)}{1 - p} + \ln(19 - 20p)\right)$$

$$K_p = \frac{1}{(1-p)}\left(\frac{2(p - .1)}{1 - p} + \ln(19 - 20p)\right) \qquad p = \frac{-V_{tp}}{V_{DD}}$$

$$t_r = K_p\frac{C_L}{k_p V_{DD}}$$

Rise time analysis

- For equal fall times and rise times

$$t_f = t_r$$

$$K_n\frac{C_L}{k_n V_{DD}} = K_p\frac{C_L}{k_p V_{DD}}$$

$$V_{tn} = V_{tp} \longrightarrow K_n = K_p$$

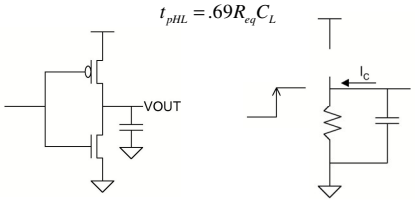
$$\mu_n C_{ox}\left(\frac{W_n}{L}\right) = \mu_p C_{ox}\left(\frac{W_p}{L}\right)$$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \approx 2-3$$

Propagation Delay

- As with interconnect delay, find the equivalent resistance and load capacitance of the transistor

$$t_{pHL} = .69R_{eq}C_L$$



Propagation Delay

$$R_{eq} = avg(R_{on}(t)) = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2}\frac{V_{DS}(t)}{I_{DS}(t)}$$

- Propagation delay is the time for voltage to reach half way point - so integrate from V_{DD} to $V_{DD}/2$

$$R_{eq} = \frac{1}{V_{DD}/2 - V_{DD}}\int_{V_{DD}}^{V_{DD}/2}\frac{V_{DS}(t)}{I_{DS}(t)}dV_{DS}$$

- For the output range we are interested in, the transistor is always in saturation

$$R_{eq} = \frac{-2}{V_{DD}}\int_{V_{DD}}^{V_{DD}/2}\frac{V_{DS}}{I_{DSAT}(1+\lambda V_{DS})}dV_{DS}$$

Propagation Delay

$$R_{eq} = \frac{-2}{V_{DD}}\int_{V_{DD}}^{V_{DD}/2}\frac{V_{DS}}{I_{DSAT}(1+\lambda V_{DS})}dV_{DS}$$

$$= \frac{2}{V_{DD}\lambda^2 I_{SAT}}(\lambda V_{DS} - \ln(1+\lambda V_{DS}))\Big|_{V_{DD}/2}^{V_{DD}}$$

$$= \frac{2}{V_{DD}\lambda^2 I_{SAT}}\left(\lambda V_{DS} - \left(\lambda V_{DS} - \frac{\lambda^2 V_{DS}^{\ 2}}{2} + \frac{\lambda^3 V_{DS}^{\ 3}}{3} - \cdots\right)\right)\Bigg|_{V_{DD}/2}^{V_{DD}}$$

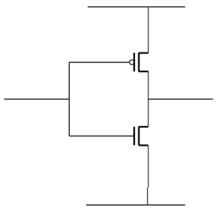
$$= \frac{2}{V_{DD} I_{SAT}}\left(\frac{V_{DS}^{\ 2}}{2} - \frac{\lambda V_{DS}^{\ 3}}{3} + \cdots\right)\Bigg|_{V_{DD}/2}^{V_{DD}}$$

$$= \frac{2}{V_{DD} I_{SAT}}\left(\frac{3V_{DD}^{\ 2}}{8} - \frac{7\lambda V_{DD}^{\ 3}}{24} + \cdots\right)$$

$$\approx \frac{3}{4}\frac{V_{DD}}{I_{SAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

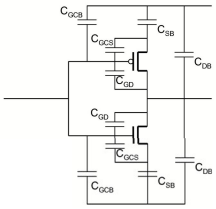
Propagation Delay

- **Load capacitance**



Propagation Delay

- **Load capacitance**
  - Intrinsic capacitance - sum of capacitances at drain - C_{GD}+ C_{DB}



Propagation Delay

- **Intrinsic capacitance**
  - C_{GD} is composed solely of overlap capacitance
    - The transistors are either in cutoff or in saturation, so no channel capacitance exists
  - The actual load capacitance relative to ground is $2C_{GDO}$ because of Miller effect
    - **Miller effect** accounts for an increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of capacitance between the input and output terminals

Propagation Delay

$$t_{pLH} = 0.69 R_{eq}(2C_{GDOn} + 2C_{GDOp} + C_{DBn} + C_{DBp} + C_{ext})$$

- Extrinsic capacitance is composed of wire capacitance and input capacitance of fanout
- Input capacitance is composed of overlap capacitance and channel capacitance
  - Overlap capacitance is C_{GDO} + C_{GSO} (very small)
  - Channel capacitance is C_{ox}WL. Assume worst case

Propagation Delay

- All capacitances are roughly proportional to W
- Equivalent resistance is inversely proportional to W