Topics

- Performance Characterization
  - Resistance Estimation
  - Capacitance Estimation
  - Inductance Estimation

Performance Characterization

- Voltage versus Time curve (ideal)

Performance Characterization

- Gate delay
- Voltage versus Time curve

Performance Characterization

- Interconnect delay

Performance Characterization

- Delay
  - Primary determinant of the speed of a circuit
  - Due to resistances and capacitances

Resistance Estimation

- Dependent on resistivity $\rho$ of material
- Directly proportional to length
- Inversely proportional to cross-sectional area

\[ R = \rho \frac{l}{A} \]
Resistance Estimation

\[ R = \rho \frac{L}{A} = \rho \frac{L}{W} = R_s \frac{L}{W} \]

- \( R_s \) is the sheet resistance expressed in terms of \( \Omega/\square \) (ohms per square)
- square is a dimensionless quantity

Resistance Estimation

<table>
<thead>
<tr>
<th>Interconnect Material</th>
<th>Typical Resistance ((\Omega/\square))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top metal (Al)</td>
<td>0.05-0.1</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>150-200</td>
</tr>
<tr>
<td>Diffusion</td>
<td>50-150</td>
</tr>
</tbody>
</table>

(Based on a typical 0.25 \(\mu\)m CMOS process)

Resistance Estimation

- Intrinsic resistance
- In linear region (for a given \( V_{GS} \))

\[ I_{in} = \frac{V_{GS} - V_T}{2} \]

\[ R_{in} = \frac{1}{k(V_{GS} - V_T)} = \frac{1}{\mu C_{ox} V_T} \frac{1}{W} \frac{V_{GS} - V_T}{L} \]

\[ R_s = \frac{1}{\mu C_{ox} (V_{GS} - V_T)} \]

Capacitance Estimation

- Intrinsic capacitance
- Interconnect capacitance
- Interconnect capacitance and resistance is the primary determinant of interconnect delays
MOS device capacitances

- Overlap related capacitance
- Channel related capacitances
  - Dependent on region of operation
  - Diffusion to substrate capacitances

Overlap related capacitance

\[ C_{GDS} = C_{GOO} = \frac{\varepsilon_o A_{\text{overlap}}}{t_{ox}} = \frac{C_{ox} x_D W}{L_x} \]

- Usually can be ignored since \( x_D \) is very small

Channel related capacitances

- Cutoff
  - No channel
  - Therefore, no gate to source or drain capacitances

Channel related capacitances

- Depletion -- No channel

\[ C_{GDS} = C_{GOO} = \frac{C_{ox} C_{W/L}}{C_{ox} + C_{W/L}} = \frac{C_{W/L} x_D}{W/L} \]

\( C_{ox} \)
Channel related capacitances

As gate voltage increases, depletion region deepens (d increases), causing $C_{dep}$ to decrease, and thus decrease the gate to body capacitance.

As gate voltage nears $V_T$, inversion channel forms causing a barrier for the gate to body capacitance.

Saturation

- Channel is pinched off
- Gate to source capacitance exists
- Gate to drain capacitance is zero

$$C_{GCS} = \frac{2}{3}C_{WL}$$

$$C_{GCD} = 0$$

Channel related capacitances

Linear

- Channel is formed
- Therefore, no gate to body capacitance

$$C_{GCS} = C_{GCD} = \frac{C_{WL}}{2}$$

Transistor Grate Capacitance

Channel related capacitances

Worst case

- $C_{ox}$ ranges from 1.7-6 fF/µm²
- For a 1.5µ by 1.5µ channel

$$C_x = (6)(1.5)(1.5)$$

$$= 13.5 \text{ fF}$$
MOS device capacitances

- Diffusion to substrate capacitance
- Junction capacitance

\[ C_{j} = C_{jSW} + C_{jdiff} \]

- \( C_{j} \) is the bottom-plate capacitance per area

MOS device capacitances

- Side wall or periphery capacitance (drain and source sidewalls)

\[ C_{jSW} = C_{jSW}(2L_{s} + W) \]

- \( C_{jSW} \) is the side wall capacitance per linear distance

MOS device capacitances

- \( C_{j} \) is typically 0.5 - 2 fF/\( \mu m^2 \)
- \( C_{jSW} \) is typically 0.28 - 0.4 fF/\( \mu m \)
- For a 1.5\( \mu m \) by 1.5\( \mu m \) diffusion region

\[ C_{eff} = C_{jSW} + C_{jdiff} \]

\[ C_{eff} = 2(1.5)l(3.0) + 28(3.0 + 1.5) \]

\[ C_{eff} = 58 fF \]

Interconnect capacitances

- When \( h \) is comparable in magnitude to \( t \), fringing electric fields can increase the total effective parasitic capacitance
- The effect is magnified as the ratio of \( w \) to \( h \) decreases
- If \( w = h \), the effective capacitance can be up to 10 times \( C_{plate} \)

Cross-Interconnect capacitances

- Can be very difficult to compute
- Requires three dimensional field simulations
- Usually provided by process measurements
Cross-Interconnect capacitances

<table>
<thead>
<tr>
<th>Process</th>
<th>Area ($\mu m^2$)</th>
<th>Perimeter ($\mu m$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly over oxide</td>
<td>0.988</td>
<td>0.054</td>
</tr>
<tr>
<td>Metall1 over oxide</td>
<td>0.030</td>
<td>0.010</td>
</tr>
<tr>
<td>Metall2 over oxide</td>
<td>0.013</td>
<td>0.025</td>
</tr>
<tr>
<td>Metall1 over poly</td>
<td>0.057</td>
<td>0.054</td>
</tr>
<tr>
<td>Metall2 over poly</td>
<td>0.017</td>
<td>0.029</td>
</tr>
<tr>
<td>Metall2 over Metall1</td>
<td>0.036</td>
<td>0.045</td>
</tr>
</tbody>
</table>

Inductance

- For the most part is not an issue
- Small enough to ignore except for very high performance chips
- Inductance is usually higher for I/O interfaces

Delay Definitions

Interconnect delay

- Lumped RC model
- Charge $V_{in}$ to $V_{DD}$
- The transient output voltage is
  \[ V_{out}(t) = V_{DD} \left( 1 - e^{-\frac{t}{RC}} \right) \]
  \[ t_{delay} = \frac{V_{DD}}{2} \left( 1 - e^{-\frac{t}{RC}} \right) \]
  \[ t_{delay} = \frac{69}{2} RC \]

- More accurate than lumped RC model
- More difficult to solve for large $N$
- Need full-scale SPICE simulation