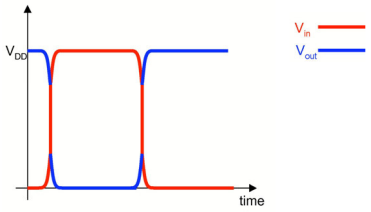
Topics

- Performance Characterization
  - Resistance Estimation
  - Capacitance Estimation
  - Inductance Estimation

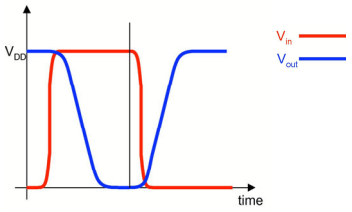
Performance Characterization

- Voltage versus Time curve (ideal)



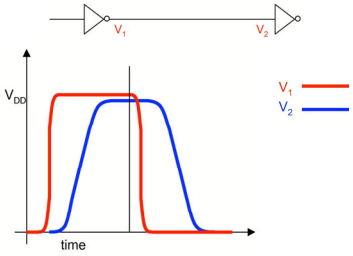
Performance Characterization

- Gate delay
- Voltage versus Time curve



Performance Characterization

- Interconnect delay



Performance Characterization

- Delay
  - Primary determinant of the speed of a circuit
  - Due to resistances and capacitances

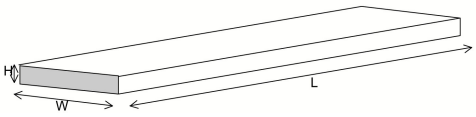
Resistance Estimation

- Dependent on resistivity ρ of material
- Directly proportional to length
- Inversely proportional to cross-sectional area

$$R = \rho \frac{l}{A}$$

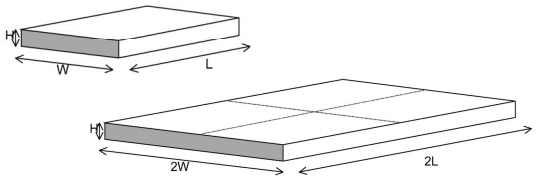
Resistance Estimation

$$R = \rho \frac{l}{A} = \frac{\rho}{H} \frac{l}{W} = R_s \frac{L}{W}$$



Resistance Estimation

- R_s is the sheet resistance expressed in terms of Ω/ (ohms per square)
  - square is a dimensionless quantity



Resistance Estimation

Interconnect Material	Typical Resistance (Ω/□)
Top metal (Al)	0.05-0.1
Polysilicon	150-200
Diffusion	50-150

(Based on a typical 0.25 µm CMOS process)

Resistance Estimation

- Intrinsic resistance
- In linear region (for a given V_{GS})

$$I_{DS} = k\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$R_{eq} = \frac{1}{k(V_{GS} - V_T)} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)} = \frac{1}{\mu C_{ox}(V_{GS} - V_T)} \frac{L}{W}$$

$$R_s = \frac{1}{\mu C_{ox}(V_{GS} - V_T)}$$

Resistance Estimation

- Intrinsic resistance
  - Dependent on C_{ox} and carrier mobility
  - Typically 1000-3000 Ω/
  - Temperature variant

$$R_s = \frac{1}{\mu C_{ox}(V_{GS} - V_T)}$$

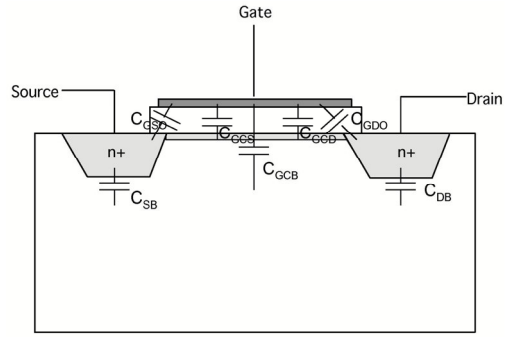
Capacitance Estimation

- Intrinsic capacitance
- Interconnect capacitance
- Interconnect capacitance and resistance is the primary determinant of interconnect delays

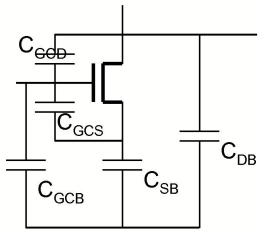
MOS device capacitances

- Overlap related capacitance
- Channel related capacitances
  - Dependent on region of operation
- Diffusion to substrate capacitances

MOS device capacitances



MOS device capacitances

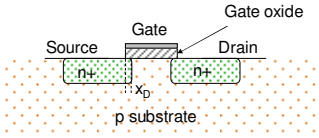


MOS device capacitances

Overlap related capacitance

$$C_{GSO} = C_{GDO} = \frac{\varepsilon_{ox}}{t_{ox}} A_{overlap} = C_{ox} x_D W$$

- Usually can be ignored since x_D is very small



MOS device capacitances

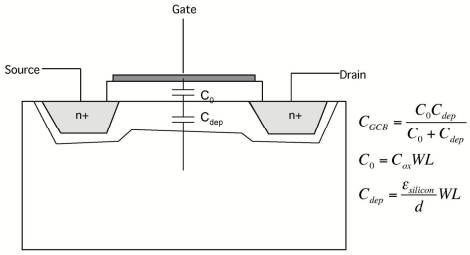
Channel related capacitances

- Cutoff
  - No channel
  - Therefore, no gate to source or drain capacitances

MOS device capacitances

Channel related capacitances

Depletion -- No channel



$$C_{GCB} = \frac{C_0 C_{dep}}{C_0 + C_{dep}}$$

$$C_0 = C_{ox} WL$$

$$C_{dep} = \frac{\varepsilon_{silicon}}{d} WL$$

MOS device capacitances

Channel related capacitances

- As gate voltage increases, depletion region deepens (d increases), causing C_{dep} to decrease, and thus decrease the gate to body capacitance
- As gate voltage nears V_T, inversion channel forms causing a barrier for the gate to body capacitance

MOS device capacitances

Channel related capacitances

- Saturation
  - Channel is pinched off
  - Gate to source capacitance exists
  - Gate to drain capacitance is zero

$$C_{GCS} = \frac{2}{3} C_{ox} WL$$

$$C_{GCD} = 0$$

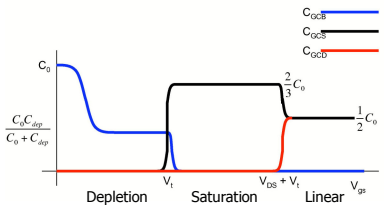
MOS device capacitances

Channel related capacitances

- Linear
  - Channel is formed
  - Therefore, no gate to body capacitance

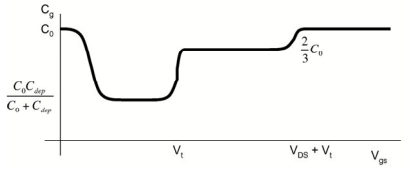
$$C_{GCS} = C_{GCD} = \frac{C_{ox} WL}{2}$$

MOS device capacitances



MOS device capacitances

Transistor Grate Capacitance



MOS device capacitances

- Channel related capacitances
- Worst case

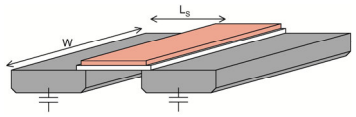
$$C_g = C_{ox} WL$$

- C_{ox} ranges from 1.7-6 fF/μm^2
- For a 1.5μ by 1.5μ channel

$$C_g = (6)(1.5)(1.5)$$
$$= 13.5\,fF$$

MOS device capacitances

- Diffusion to substrate capacitance
- Junction capacitance

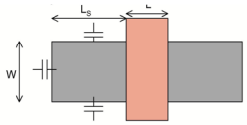


$$C_{diff} = C_j L_s W$$

- C_j is the bottom-plate capacitance per area

MOS device capacitances

- Side wall or periphery capacitance (drain and source sidewalls)



$$C_{diff} = C_{jsw}(2L_s + W)$$

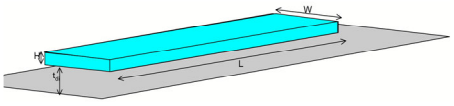
- C_{jsw} is the side wall capacitance per linear distance

MOS device capacitances

- C_j is typically 0.5 - 2 fF/μm^2
- C_{jsw} is typically 0.28 - 0.4 fF/μm
- For a 1.5μ by 1.5μ diffusion region

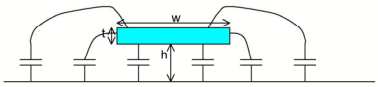
$$\begin{aligned} C_{diff} &= C_j L_s W + C_{jsw}(2L_s + W) \\ &= 2(1.5)(1.5) + .28(3.0 + 1.5) \\ &= 5.8\,fF \end{aligned}$$

Interconnect capacitances



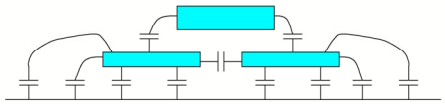
$$C_{plate} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Interconnect capacitances



- When h is comparable in magnitude to t, fringing electric fields can increase the total effective parasitic capacitance
- The effect is magnified as the ratio of w to h decreases
- If w=h, the effective capacitance can be up to 10 times C_{plate}

Cross-Interconnect capacitances



- Can be very difficult to compute
- Requires three dimensional field simulations
- Usually provided by process measurements

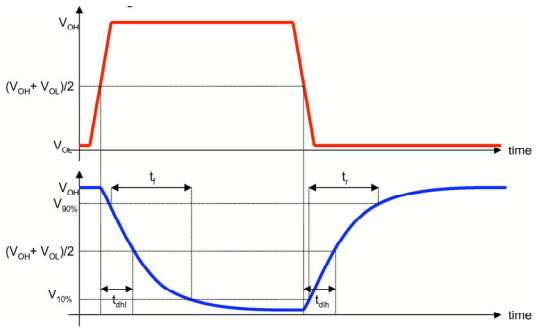
Cross-Interconnect capacitances

.25μm process	Area (fF/μm²)	Perimeter (fF/μm)
Poly over oxide	.088	.054
Metal1 over oxide	.030	.040
Metal2 over oxide	.013	.025
Metal1 over poly	.057	.054
Metal2 over poly	.017	.029
Metal2 over Metal1	.036	.045

Inductance

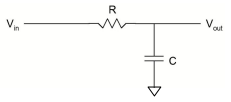
- For the most part is not an issue
- Small enough to ignore except for very high performance chips
- Inductance is usually higher for I/O interfaces

Delay Definitions



Interconnect delay

- Lumped RC model



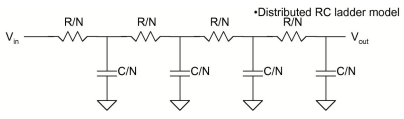
- Charge V_{in} to V_{DD}
- The transient output voltage is $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$

$$\frac{V_{DD}}{2} = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$$

$$\frac{t_{dlh}}{RC} = -\ln\left(\frac{1}{2}\right)$$

$$t_{dlh} \approx .69RC$$

Interconnect delay



- More accurate than lumped RC model
- More difficult to solve for large N
- Need full-scale SPICE simulation