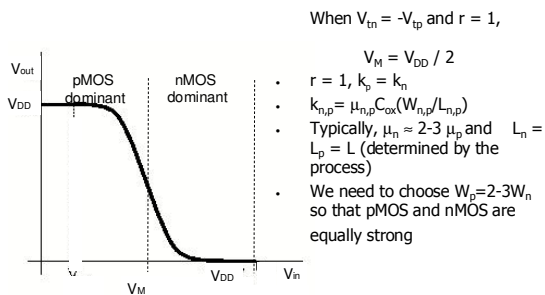


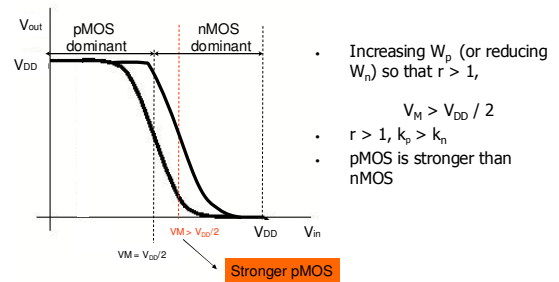
## Transistor Strength



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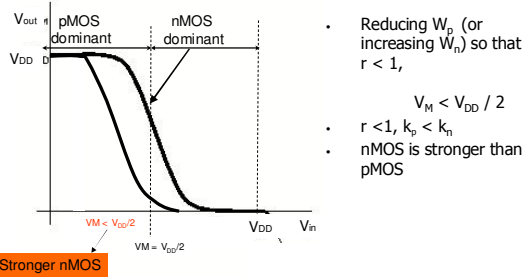
## Transistor Strength



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## Transistor Strength



3 March 2009

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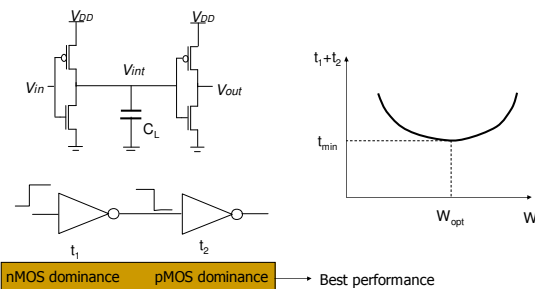
## Performance Tradeoffs

- By increasing the width, we can make a transistor stronger (faster)
- Can we make an arbitrarily large transistor for arbitrarily high performance?
- No! Because there are other constraints!

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## Performance Tradeoffs

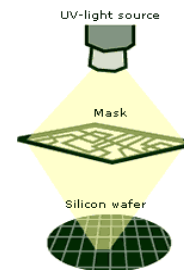


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## Semiconductor Processing

- How do we make a transistor?

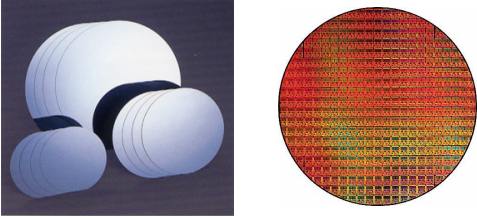


- How do you control where the features get placed?
  - Photo lithography masks

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## Wafer Processing



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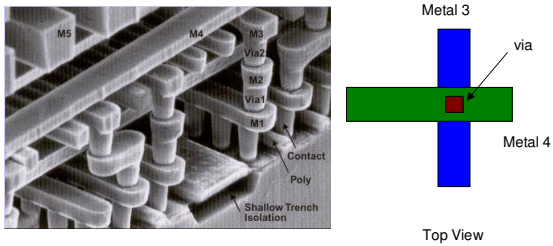
## Interconnect

- Polysilicon to Metal contacts
- Diffusion to Metal contacts
- Metal to Metal vias

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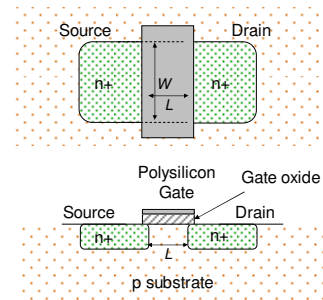
## Metallization



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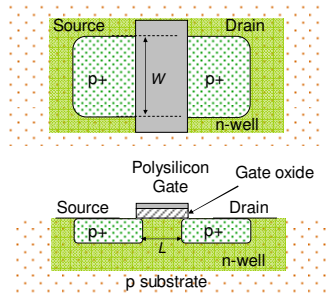
## nMOS Structure



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## pMOS Structure



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## CMOS Process Layers

Layer Description	Representation
metal	m1, m2, m3, m4, m5
well	w1
polysilicon	poly
contacts & vias	ct, v12, v23, v34, v45
active area and P&T's	ndif, pdif

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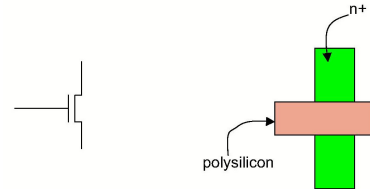
## Semiconductor Masks



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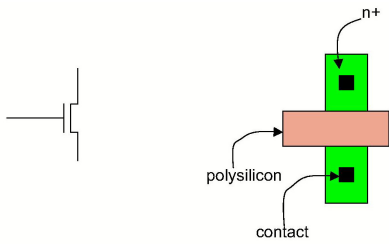
## Semiconductor Masks



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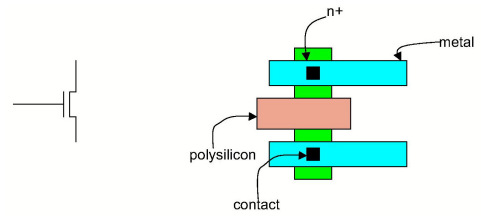
## Semiconductor Masks



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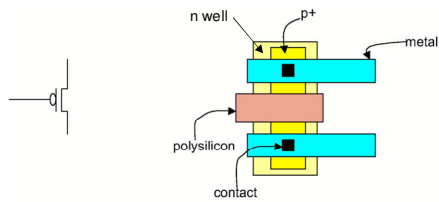
## Semiconductor Masks



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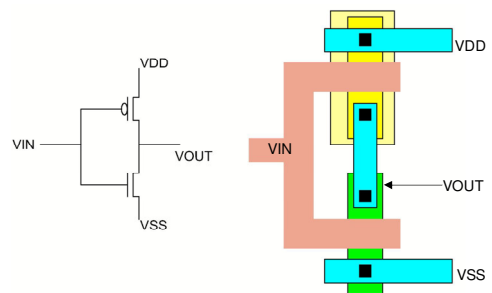
## Semiconductor Masks



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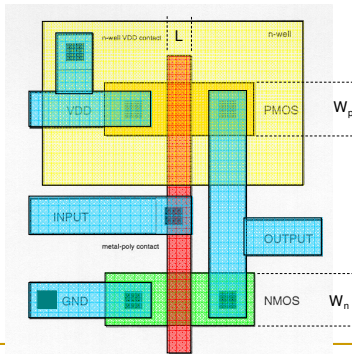
## Semiconductor Masks



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## Layout Optimization



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## Design rules

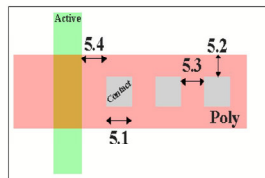
- Design rules are critical to proper operation of the circuit
- They place restrictions on the sizes of layers and the distance between layers
- Often expressed in terms of  $\lambda$  - half the minimum feature size

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## Design rules

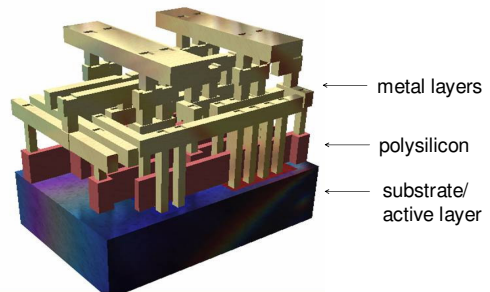
MOSIS SCMOS Design Rules		
5.1	Contact size	2x2
5.2	Minimum poly overlap	1.5
5.3	Minimum contact spacing	2
5.4	Minimum spacing to gate of transistor	2



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## Fabrication



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