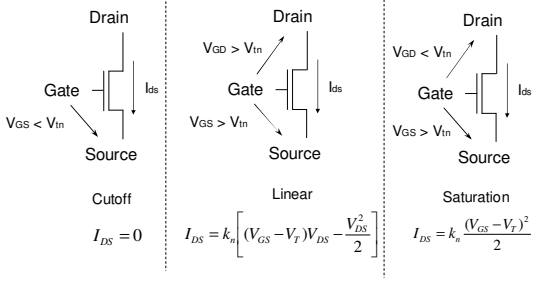
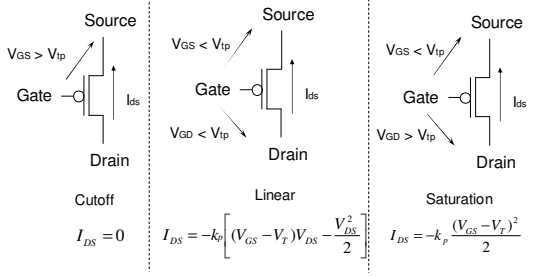
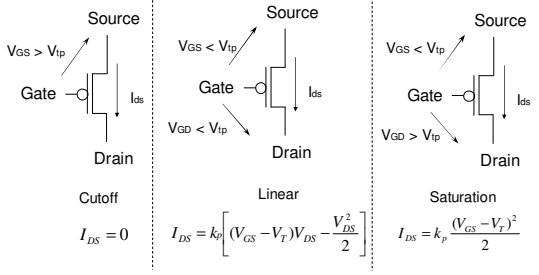
Operation Mode: nMOS



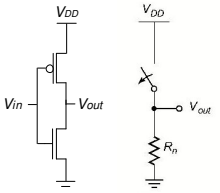
Operation Mode: pMOS



Operation Region: pMOS



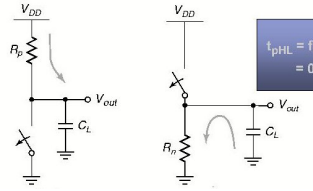
CMOS Inverter First-Order DC Analysis



$V_{OL} = 0$
$V_{OH} = V_{DD}$

- High noise margin
- Ratioless
- low output impedance
- extremely high input impedance
- no static power

CMOS Inverter: Transient Response



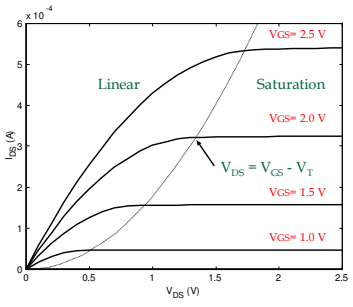
$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

To reduce delay:
- Reduce CL
- Reduce Rp,n
- Increase W/L ratio

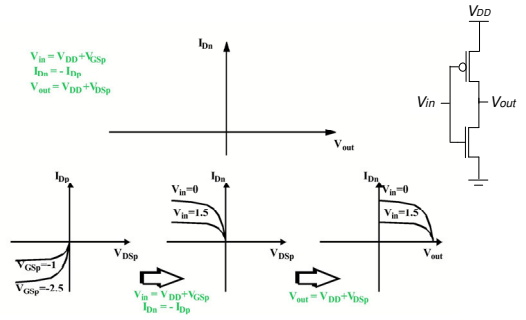
Output: Low-to-High High-to-Low

CL is composed of the drain diffusion capacitances of the NMOS and PMOS transistors, the capacitance of connecting wires, and the input capacitance of the fan-out gates

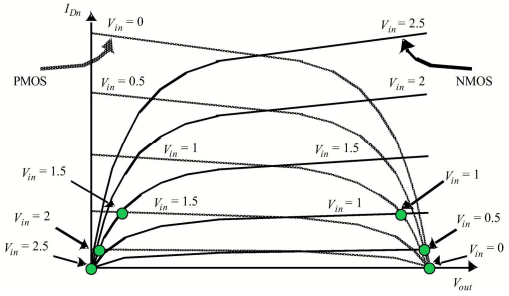
NMOS Load Lines



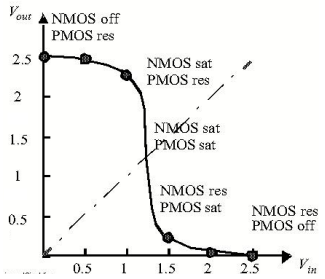
PMOS Load Lines



CMOS Inverter Load Characteristics

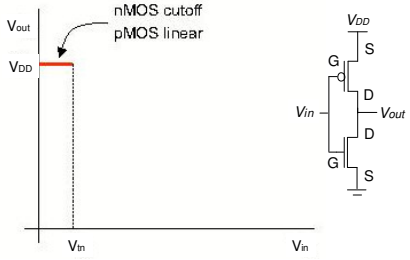


CMOS Inverter VTC

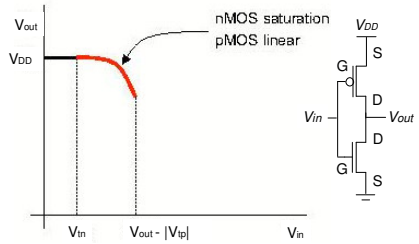


VTC: Voltage-Transfer Characteristic

CMOS Inverter VTC



CMOS Inverter VTC



CMOS Inverter VTC

- Set pMOS Linear I_{DS} equal to nMOS Saturation I_{DS}

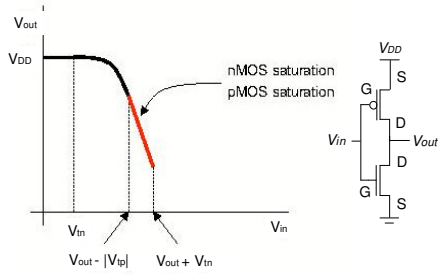
$$k_n\left(\frac{(V_{in}-V_{tn})^2}{2}\right)=k_p\left((V_{in}-V_{DD}-V_{tp})(V_{out}-V_{DD})-\frac{(V_{out}-V_{DD})^2}{2}\right)$$

$$\frac{(V_{out}-V_{DD})^2}{2}-(V_{in}-V_{DD}-V_{tp})(V_{out}-V_{DD})+\frac{k_n}{k_p}\frac{(V_{in}-V_{tn})^2}{2}=0$$

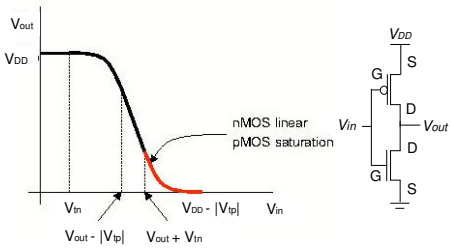
$$(V_{out}-V_{DD})=(V_{in}-V_{DD}-V_{tp})+\sqrt{(V_{in}-V_{DD}-V_{tp})^2-\frac{k_n}{k_p}(V_{in}-V_{tn})^2}$$

$$V_{out}=(V_{in}-V_{tp})+\sqrt{(V_{in}-V_{DD}-V_{tp})^2-\frac{k_n}{k_p}(V_{in}-V_{tn})^2}$$

CMOS Inverter VTC



CMOS Inverter VTC



CMOS Inverter VTC

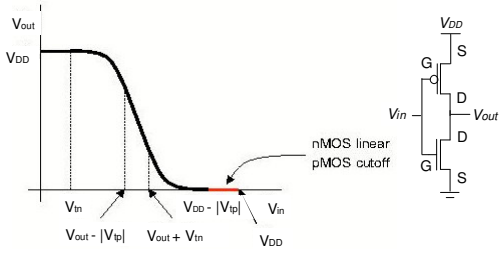
- Set nMOS Linear I_{DS} equal to pMOS Saturation I_{DS}

$$k_p\left(\frac{(V_{in}-V_{DD}-V_{tp})^2}{2}\right)=k_n\left((V_{in}-V_{tn})V_{out}-\frac{V_{out}^2}{2}\right)$$

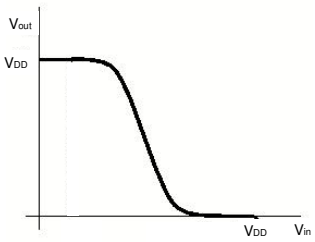
$$\frac{V_{out}^2}{2}-(V_{in}-V_{tn})V_{out}+\frac{k_p}{k_n}\frac{(V_{in}-V_{DD}-V_{tp})^2}{2}=0$$

$$V_{out}=(V_{in}-V_{tn})-\sqrt{(V_{in}-V_{tn})^2-\frac{k_p}{k_n}(V_{in}-V_{DD}-V_{tp})^2}$$

CMOS Inverter VTC



CMOS Inverter VTC



CMOS Inverter

(assume $V_t = V_{tn} = |V_{tp}|$)

V_{in}	pMOS mode	nMOS mode	V_{out}
$V_{in} < V_t$	Linear	Cutoff	V_{DD}
$V_t < V_{in} < V_{out} - V_t$	Linear	Saturation	$(V_{in}+V_t)+\sqrt{(V_{in}-V_{DD}+V_t)^2-(V_{in}-V_t)^2}$
$V_{out}-V_t < V_{in} < V_{out}+V_t$	Saturation	Saturation	Interpolate
$V_{out}+V_t < V_{in} < V_{DD}-V_t$	Saturation	Linear	$(V_{in}-V_t)-\sqrt{(V_{in}-V_t)^2-(V_{in}-V_{DD}+V_t)^2}$
$V_{in} > V_{DD}-V_t$	Cutoff	Linear	0

Switching Threshold

- The point (V_m) at which the inverter has both transistors in saturation ($V_{in} = V_{out}$)

$$\frac{k_n}{2}(V_M - V_{in})^2 = \frac{k_p}{2}(V_M - V_{DD} - V_{tp})^2$$

$$(V_M - V_{in}) = -\sqrt{\frac{k_p}{k_n}}(V_M - V_{DD} - V_{tp})$$

r

$$V_M(1+r) = V_{in} + r(V_{DD} + V_{tp})$$

$$V_M = \frac{V_{in} + r(V_{DD} + V_{tp})}{1+r}$$

r is the relative driving strengths of the PMOS and NMOS transistors

Switching Threshold

$$V_M = \frac{V_{in} + r(V_{DD} + V_{tp})}{1+r}$$

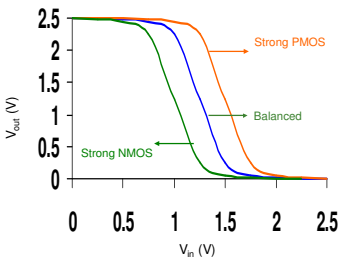
- When $V_{tn} = -V_{tp}$ and $r = 1$,

$$V_M = \frac{V_{DD}}{2}$$

- When $V_{tn} = -V_{tp}$ and $r > 1$,

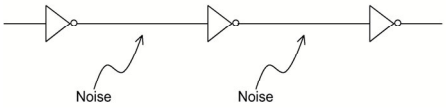
$$V_M > \frac{V_{DD}}{2} \longrightarrow \text{Stronger PMOS}$$

Switching Threshold

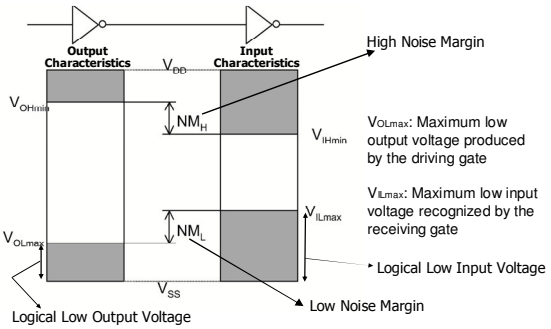


Noise Margin

- A measure of the acceptable noise at a gate input so that the output is not affected.
- Noise margin is closely related to the DC voltage characteristics
- Sources: supply noise, crosstalk, interference



Noise Margin



V_OLmax: Maximum low output voltage produced by the driving gate

V_IHmin

Noise Margins

- Voltage Transfer Function

$$V_{out} = f(V_{in})$$

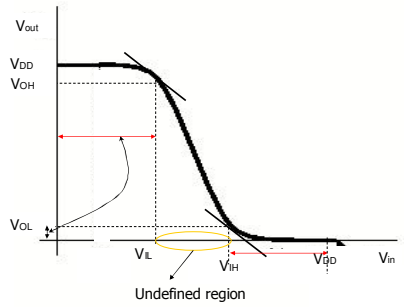
- Voltage Transfer Function with Noise

$$V_{out} = f(V_{in} + \Delta V_{noise})$$

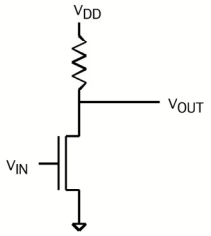
$$V_{out} \approx f(V_{in}) + \frac{dV_{out}}{dV_{in}}\Delta V_{noise}$$

- Perturbed voltage is the sum of the nominal output plus the gain times the noise
- Keep the gain less than 1

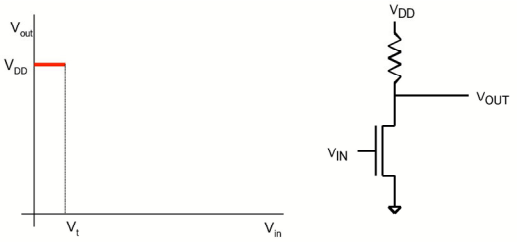
Noise Margins



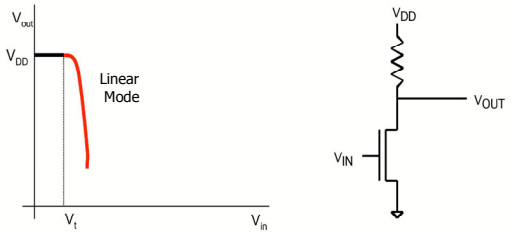
Static Load Inverter



Static Load Inverter



Static Load Inverter



Static Load Inverter

- Transistor is in linear region

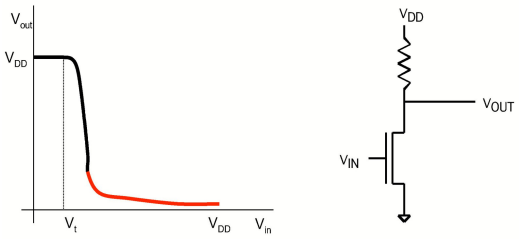
$$I_{DS} = k_n\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$V_{OUT} = V_{DD} - Rk_n\left[(V_{IN} - V_T)V_{OUT} - \frac{V_{OUT}^2}{2}\right]$$

$$\frac{Rk_n}{2}V_{OUT}^2 - (Rk_n(V_{IN} - V_T) + 1)V_{OUT} + V_{DD} = 0$$

$$V_{OUT} = (V_{IN} - V_T) + \frac{1}{Rk_n} - \sqrt{\left((V_{IN} - V_T) + \frac{1}{Rk_n}\right)^2 - 2\frac{V_{DD}}{Rk_n}}$$

Static Load Inverter



Static Load Inverter

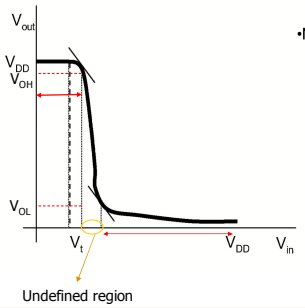
- Transistor is in saturation

$$I_{DS} = k_n \frac{(V_{GS} - V_T)^2}{2}(1 + \lambda V_{DS})$$

$$V_{OUT} = V_{DD} - Rk_n \frac{(V_{IN} - V_T)^2}{2}(1 + \lambda V_{OUT})$$

$$V_{OUT} = \frac{2V_{DD} - Rk_n (V_{IN} - V_T)^2}{2 + \lambda Rk_n (V_{IN} - V_T)^2}$$

Static Load Inverter



Undefined region

•Noise Margin

$$V_{IL} = V_T + \frac{1}{k_n R}$$

$$V_{IH} = V_T + \sqrt{\frac{8}{3}\frac{V_{DD}}{k_n R}} - \frac{1}{k_n R}$$

Static Load Inverter

- Does not go down all the way to 0 due to the resistance path between V_{DD} and ground when nMOS is on
- Static power
- Noise margins are tighter
- Switching threshold is not centered
- To get high gain in the transition region, bigger resistors are needed