MOS Transistor Theory

- Two types of transistors
  - nMOS
  - pMOS

- Digital integrated circuits use these transistors essentially as a voltage controlled switch

nMOS Transistor

- If the gate is "high", the switch is on
- If the gate is "low", the switch is off

\[
\begin{align*}
\text{Drain} & \quad g=1 \\
\text{Gate} & \quad g=0 \\
\text{Source} & \quad g=0
\end{align*}
\]

nMOS Transistor

Silicon Dioxide (SiO\textsubscript{2})

Cross-section of an n-type transistor

nMOS Transistor

- \( n \) areas have been doped with donor ions of concentration \( N_D \) - electrons are the majority carriers
- \( p \) areas have been doped with acceptor ions of concentration \( N_A \) - holes are the majority carriers
nMOS Transistor

Accumulation Mode

Depletion Mode

Inversion Mode

n-channel enhancement MOS
Threshold Voltage

- Dependent on
  - Gate conductor material
  - Gate insulator material
  - Channel Doping
  - Voltage difference between source and body

\[ V_T = V_{th} + \gamma \sqrt{2\Phi_F + V_{gs} - \sqrt{2\Phi_F}} \]

- \( \gamma \) is the body-effect coefficient and controls the impact of the source to bulk voltage
- \( \Phi_F \) is the Fermi potential and is dependent on doping levels
- Fermi potential: potential difference between Fermi level and intrinsic Fermi level in the bulk of semiconductor.
  \[ \Phi_F = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right) \]
  \( k \): Boltzmann constant, \( T \): temperature, \( q \): unit (electron) charge

pMOS Transistor

Accumulation Mode

Source vs. Drain

- nMOS: node with a higher voltage is drain, \( V_D > V_S \)
- pMOS: node with a higher voltage is source, \( V_S > V_D \)

nMOS Transistor

Linear mode

Source vs. Drain

- nMOS: node with a higher voltage is drain, \( V_D > V_S \)
- pMOS: node with a higher voltage is source, \( V_S > V_D \)
nMOS Transistor

Drain
Gate
Source

V_GS> V_T
V_GS = V_D - V_T
V_GS < V_T

Saturation mode

MOS Transistor Characteristics

Linear Mode:
• V_GS>V_T and V_GD>V_T
• Assume that V_T is constant

\[ I_{ds} = k_i \left( \frac{(V_GS - V_T)W}{L} \right)^2 \]

• k_i = (\mu C_Ox) is called the process transconductance parameter
• Gain factor of nMOS: \( k_i = k_n'\frac{W}{L} \)

Example

- \( \mu_n = 600 \, \text{cm}^2/\text{V} \cdot \text{s} \)
- \( C_Ox = 7 \times 10^{-8} \, \text{F/cm}^2 \)
- \( W = 20 \, \mu\text{m} \)
- \( L = 2 \, \mu\text{m} \)
- \( K_n = \mu_n C_Ox \frac{W}{L} = 0.42 \, \text{mA/V}^2 \)

In Summary

- Cutoff region (V_GS< V_T)
- Linear region (V_GS>V_T, V_D<V_GS-V_T or V_GD>V_T)
  \[ I_{ds} = k_i \left( \frac{(V_GS - V_T)W}{L} \right)^2 \]
- Saturated region (V_GS>V_T, V_D>V_GS-V_T or V_GD<V_T)
  \[ I_{ds} = k_i \left( \frac{(V_GS - V_T)W}{L} \right)^2 \]

I-V Characteristics

- \( V_GS = 2.5 \, \text{V} \)
- \( V_GS = 2.0 \, \text{V} \)
- \( V_GS = 1.5 \, \text{V} \)
- \( V_GS = V_GS - V_T \)

Long channel transistor (L = 10\mu m)
### MOS Transistor

- **Cutoff region** ($V_{GS} < V_T$)
  
  ![](https://example.com/cutoff_region_diagram.png)

- **Linear region** ($V_{GS} > V_T, V_{DS} < V_{GS} - V_T$)
  
  ![](https://example.com/linear_region_diagram.png)

- **Saturated region** ($V_{GS} > V_T, V_{DS} > V_{GS} - V_T$)
  
  ![](https://example.com/saturated_region_diagram.png)

### Secondary Effects

- **Body effect**
- **Channel-length modulation**
- **Drain punch-through**
- **Short channel effect**
- **Velocity saturation**

### Body Effect

- We assumed that $V_{SB} = 0$ - i.e. the source potential equals the substrate potential
- In certain situations, this assumption is not true
- Has the effect of raising the threshold voltage
  - A negative bias on the well or substrate causes the threshold to increase

### Channel-Length Modulation

- We previously assumed a constant $L$
- In reality, when $V_{DS} > (V_{GS} - V_T)$, the channel is pinched off and the effective channel length is reduced.
- Net effect is that $I_{DS}$ is not constant in the saturated region.

$$I_{DS} \propto \frac{1}{L^2}$$
MOS Transistor

- Cutoff region \( V_{GS} < V_T \)
  \[ S \quad \text{T} \quad D \]

- Linear region \( V_{GS} > V_T, V_{DS} < V_{GS} - V_T \)
  \[ S \quad \text{T} \quad D \]

- Saturated region \( V_{GS} > V_T, V_{DS} > V_{GS} - V_T \)
  \[ S \quad \text{T} \quad D \]

Short Channel Effect

- At small gate lengths, electric field becomes more pronounced
- Electrons get excited with enough energy to cause a substrate current
- This causes change of transistor parameters - threshold voltage, current flow, etc.

Velocity Saturation

- Assumption was that carrier velocity is proportional to electric field
- When channel is small, and the voltage is large, the velocity can saturate
  \[ v = \begin{cases} \mu \xi & \xi < \xi_s \\ \mu \xi & \xi > \xi_s \\ \end{cases} \]
  \( \xi_s \) is value of electric field at which velocity saturates

MOS Transistor

- Cutoff region \( V_{GS} < V_T \)
  \( I_{DS} = 0 \)

- Linear region \( V_{GS} > V_T, V_{DS} < V_{GS} - V_T \)
  \[ I_{DS} = k \left[ (V_{GS} - V_T)W_{sat} - \frac{V_{DS}^2}{2} \right] \]

- Saturated region \( V_{GS} > V_T, V_{DS} > V_{GS} - V_T \)
  \[ I_{DS} = k \left[ (V_{GS} - V_T)W_{sat} - \frac{V_{DS}^2}{2} \right] \]

MOS Gain Characteristics

- Transconductance \( g_m = \frac{dI}{dV_G} \)
  - Cutoff region \( g_m = 0 \)
  - Linear region \( g_m = k \left[ V_{GS} - V_T \right] \)
  - Saturated region \( g_m = k \left[ V_{DS} - V_T \right] \)
nMOS Transistor

- Cutoff region ($V_{GSn} < V_{Thn}$)
  
  \[ I_{Dn} = 0 \]

- Linear region ($V_{GSn} > V_{Thn}$, $V_{DSn} < V_{GSn} - V_{Thn}$)

  \[ I_{Dn} = k_n \left( V_{GSn} - V_{Thn} \right) \frac{V_{DSn}^2}{2} \]

- Saturated region ($V_{GSn} > V_{Thn}$, $V_{DSn} > V_{GSn} - V_{Thn}$)

  \[ I_{Dn} = k_n \left( V_{GSn} - V_{Thn} \right)^2 \left( 1 + \lambda V_{DSn} \right) \]

pMOS Transistor

- Cutoff region ($V_{GSp} > V_{Thp}$)
  
  \[ I_{Dp} = 0 \]

- Linear region ($V_{GSp} < V_{Thp}$, $V_{DSp} > V_{GSp} - V_{Thp}$)

  \[ I_{Dp} = -k_p \left( V_{GSp} - V_{Thp} \right) \frac{V_{DSp}^2}{2} \]

- Saturated region ($V_{GSp} < V_{Thp}$, $V_{DSp} < V_{GSp} - V_{Thp}$)

  \[ I_{Dp} = -k_p \left( V_{GSp} - V_{Thp} \right)^2 \left( 1 + \lambda V_{DSp} \right) \]

Assume all variables negative!