ECE 3401 - Digital Systems Design

(also offered as CSE 3302)
Spring 2014, Tu/Th 11am-12:15pm @ ITE 127

Instructor: Prof. Mark (Mohammad) Tehranipoor
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Instructor's office hours : Tue 1-2pm, or upon appointments, @ ITEB 441.

TA: Qihang Shi
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TA's office hours : T 2-3pm @ ITE 430

Lab: **ITE C30, ITE learning center**

Course Description: Design and evaluation of control and data structures for digital systems. Hardware design languages are used to describe and design both behavioral and register transfer level architectures and control units with a microprogramming emphasis. Cover basic computer architecture, memories, digital interfacing, timing and synchronization, and microprocessor systems. (*three credits*)

Course materials can be found at:
http://www.engr.uconn.edu/~tehrani/teaching/ece3401/index.html

Prerequisites: CSE 2300 W (old number: 210W) - Digital Logic Design

References: ***Digital Systems Design Using VHDL*** by Charles H. Roth, Jr. and Lizy Kurian John**,** 2nd Edition, Thomson.

The Student's Guide to VHDL by Peter J. Ashenden, Morgan Kaufmann

Software Tools: The course is very tool-intensive. Homework will include designing and simulating some functional modules by using hardware description languages. We will use Xilinx ISE and ModelSim simulator. http://www.xilinx.com/ise/webpack

Grading:

Homeworks	20%
Midterm exam	25%
Final project design	25%
Final exam	30%

Rules: Participation in class discussion is strongly encouraged. Homework is due at the beginning of class on the due date, no extensions. Please turn off electronic devices during classes, like cell phones, MP3s, and iPods. Laptops, iPads, iPhones are allowed only when used for viewing class-related materials.

Topics:

Overview of digital systems
Combinational logic circuits and design
FPGA & CPLD
VHDL Description Of Digital Systems - Behavioral Modeling
VHDL Description Of Digital Systems - Structural Modeling
VHDL Description OF Arithmetic Functions
Sequential circuits
Sequential system design, processor datapath and control unit
Memory and timing issues
Computer design basic
Instruction set architecture
Pipeline design
Verilog basics (optional)
I/O, bus design, D/A, A/D, power issues (optional)