Layout-Aware Pattern Generation for Maximizing Supply Noise Effects on Critical Paths

Junxia Ma, Jeremy Lee and Mohammad Tehranipoor
ECE Department, University of Connecticut, CT, 06269
{junxia, jslee, tehrani}@engr.uconn.edu

***Abstract*— As technology scales, gate sensitivity to noise increases due to supply voltage scaling and limited scaling of the voltage threshold. As a result, power supply noise plays a greater role in sub-100nm technologies and creates signal integrity issues in the chip. It is vital to consider supply voltage noise effects (i) during design validation to apply sufficient guardbands to critical paths and (ii) during path delay test to ensure the performance and reliability of the chip. In this paper, a novel layout-aware pattern generation procedure for maximizing power supply noise effects on critical paths while considering local voltage drop impacts is proposed. The proposed pattern generation and validation flow is implemented on the ITC'99 b19 benchmark. Experimental results for both wire-bond and flip-chip packaging styles are presented in this paper. Results demonstrate that our proposed method is fast, significantly increases switching around the functionally testable critical paths, and induces large voltage drop on cells placed in the critical paths which results in increased path delay. The proposed method eliminates the very time consuming pattern validation phase that is practiced in industry.**

Keywords: Layout, Path delay test, Pattern generation, Power supply noise, Signal integrity

I. Introduction

Scaling technology has continued the push for more complex designs. In order to improve performance and reduce leakage, the power supply voltage has also been scaling. However, the reduced supply voltage also reduces the noise immunity, reducing signal integrity and negatively impacting performance and reliability.

Power supply noise refers to voltage spikes or droops on the power and ground distribution network. This can be induced by large currents drawn through the resistive power distribution network (PDN), creating IR-drop, or sudden changes in current, causing $L\frac{dI}{dt}$ effects. The main consequence of power supply noise is a negative impact on circuit timing and signal integrity. Supply voltage noise compromises the cell driving capability and thus slows down the cell transition, potentially violating setup and hold times and creating clock skew. All of these effects would degrade the circuit performance or potentially result in functional failure.

The sensitivity of the cell delay to the power supply noise increases as supply voltage scales and voltage threshold remains relatively constant [1]. It has been shown that a 10% voltage drop in a 180nm design increases the propagation delay of the gates by 8% [2]. In 130nm technology, a 10% variation in supply voltage causes a 30% delay variation for typical gates [3]. In 90nm technology, a 1% voltage change causes approximately 4% change in gate delay [4]. From these examples, we can see that the impact of power supply noise on cell delays is becoming increasingly significant with technology scaling.

Timing analysis is usually used to predict the performance of the design. Static timing analysis can verify the performance at different process-voltage-temperature (PVT) corners, which assumes the *same* operating points for all the gates. Generally, this results in a very conservative worst-case prediction since in practice only a small portion of the gates will experience worst-case voltage drop. However, in certain cases, it may be optimistic because it does not consider the mismatch between the supplies of the driving gates and the load gates [3]. Dynamic timing analysis is used to simulate the circuit timing performance with input patterns. However, the patterns are generated without considering the structure of the power distribution network or the physical location of the path in the layout. Therefore, it could be difficult to determine the worst possible power supply noise using patterns generated by conventional ATPG tools, which can be used to improve timing margins. To solve this problem, in this paper, a pattern generation method is proposed which can generate patterns to maximize the power supply noise effects on the critical paths by considering actual physical design information.

Several approaches have been proposed for power supply noise modeling, analysis, and estimation in recent years. Wang et al. [5] developed power noise models for array-bond chips and wire-bond chips during delay testing. The models are used to compact test vectors to meet noise or delay constraint. A vector-less analysis approach to compute the maximum path delay under power supply fluctuations is proposed in [3]. The path delay maximization problem is formulated as a constrained linear optimization problem considering the power supply noise effects. Nourani et al. [6] proposed a pattern generation method that maximized the power supply noise by maximizing the switching activity in the first few levels of logic that have lower fan-outs. It uses ATPG and power simulators to evaluate the gate-level netlist to find patterns that create maximum switching activity.

Several genetic-algorithm-based methods for finding patterns that induce maximum supply noise are proposed in [7]-[9]. In [7] and [8], randomly filled patterns are generated, then waveform simulations are performed to find the pattern that yields the largest supply noise. A combination of Monte Carlo and a genetic algorithm search for the worst-case input vector pairs that induce maximum switching noise is implemented in [9]. Timing analysis used an event-driven simulator and a delay lookup table.

Most of the previously proposed test pattern generation methods only use gate-level information and have no knowl-

1093-0167/09 $25.00 © 2009 IEEE
DOI 10.1109/VTS.2009.45

edge of the physical location of the critical paths or any other gates. The patterns generated by these methods do not necessarily result in the worst-case critical path delays nor chip performance.

In this paper, we propose a layout-aware pattern generation method to increase the switching activity around the critical paths. By increasing the switching activity of the neighboring cells around the critical paths, we can generate a pattern that maximizes supply noise effects on cells in those paths. These patterns can be used to verify design margins during validation or applied to the chip to determine performance and reliability during production test.

We use a fast and accurate method to validate the patterns we generated. Based on a commercial rail analysis tool, we perform supply noise aware spice simulation on a the targeted path to predict its path delay. This is then compared to the delays simulated on a large number of random-filled path-delay-fault (PDF) patterns. Simulation results show that, compared to random PDF patterns, the patterns generated with our method can create a much larger voltage drop and hence longer path delay.

Note that a vector pair is needed to analyze power supply noise in integrated circuits. For the sake of simplicity, in this paper, we use term pattern for vector pair.

The remainder of the paper is organized as follows. Section II discusses the localized IR-drop/ground-bounce effects and the path delay caused by these effects. Section III presents the layout-aware, TDF pattern generation procedure and experimental results are shown in Section IV. Finally, the concluding remarks will be given in Section V.

II. Supply Voltage Noise Induced Delay Analysis

Power supply noise includes two major components: inductive and resistive power/ground voltage noise. The inductive noise ($L\frac{dI}{dt}$) depends on the rate of change of the instantaneous current flowing through the power/ground distribution network, where the inductance *L* is mainly introduced by package lead and wire/substrate parasitics. The resistive noise (IR) is contributed by the current flow and the resistance of the power/ground network. Generally, the resistive voltage drop occurring on the power network is called IR-drop, while resistive or inductive voltage increase on ground network is called ground-bounce. Both IR-drop and ground bounce will decrease the operating voltage range of the chip and may result in timing problems and functional failures.

Since the inductance, *L*, and resistance, *R*, of the power/ground distribution network can be considered fixed for a given layout, large changes in current and instantaneous current tend to be the significant issues that contribute to high power supply noise. In typical CMOS integrated circuits, instantaneous current is mostly caused by gate switching. By increasing switching activity in a circuit, the current it draws from the PDN will also increase; also increasing voltage drop. Although our method can potentially increase the inductive noise as well, in this paper we only focus on the resistive noise increase, i.e. *total IR-drop on both power and ground networks*. The effective voltage drop for each cell equals the voltage drop on cell's power pin and voltage increase on cell's ground pin.

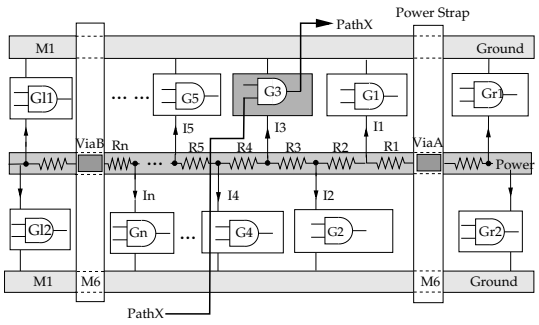

Fig. 1. A local resistive power distribution network in a standard cell design. Cell *G3* is part of the critical path *PathX*.

A. Localized Voltage Drop Analysis

In standard-cell based designs, cells are typically placed in rows and power is distributed among cells by power and ground rails on the top and bottom of each cell. As the cells are placed side-by-side, this will form a single rail across the row. Supply rails are usually routed in lower level metal layers (Metal 1 or Metal 2, depending on the supply design strategy used in the standard cell library) and are connected to the global power distribution network in the upper layers by power vias. The global PDN in upper level metal layers may have different structures and resistive properties for different designs. However, their resistive properties in local PDN are similar. Figure 1 illustrates a typical standard cell layout with cells placed in rows and power and ground rails tied horizontally to the cells. Rows are placed back-to-back and share a common power rail. Power and ground rails are routed in Metal 1 and connected to Metal 6 through vias (e.g. *ViaA, ViaB*). Figure 1 also shows part of a critical path going through this region. Cell *G3* of this critical path is placed in between the power and upper ground power rails as shown in the figure. Knowledge of the surrounding cells that share the same supply rails will be a vital part of local IR-drop analysis.

Assuming cell *G4* is the only switching cell, consuming current *I4*, and no other gates will be drawing current from the supply rails in this region, *ViaA* and *ViaB* will supply most, if not all, of the current required for cell *G4*. Current *I4* can be broken down into two basic current components, current drawn from the left of *G4*, I_{4L}, and current drawn from the right of *G4*, I_{4R}. The amount of current drawn through each via depends on the distance (i.e. resistance) between the switching cell and the via. Due to the current drawn by cell G4 flowing through the power rail, the neighboring cells will also experience voltage drop. For example, cell *G3* will see voltage drop of $I_{4R}(R_{global} + R_1 + R_2 + R_3)$ because of the current drawn by cell G4 through *ViaA* and other neighboring vias from the right side of *ViaA*. Here, R_{global} is the resistance of the global PDN in the top layer metals between power pads/C4 bumps to *ViaA*. The same analysis would apply for voltage drop on cells located to the left of cell *G4*.

Simulations have been performed to analyze localized IR-drop effects caused by switching cells that are in close prox-

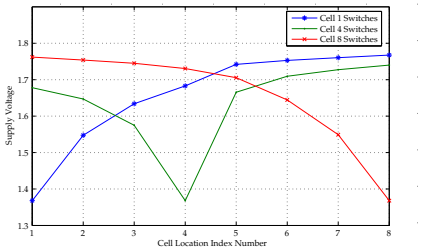

Fig. 2. The local IR-drop effect caused by single cell switching.

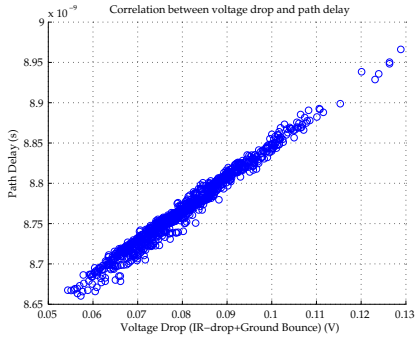

Fig. 3. Correlation between voltage drop (IR-drop + Ground-bounce) and path delay for one path in *b19* benchmark for 1000 random Path-Delay-Fault patterns; correlation coefficient is 0.99.

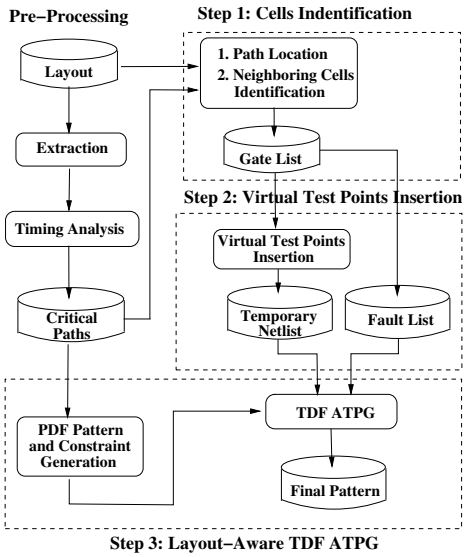

Fig. 4. Flow diagram maximizing power supply noise around critical paths using layout-aware pattern generation.

imity to one another. Figure 2 illustrates the supply voltage variation for eight adjacent cells that are connected to the same power rail with a single cell switching. This figure shows the voltage drops on each cell in the row when cell 1 (closest to left strap), cell 4 (in the middle of the row), and cell 8 (closest to right strap) switch. The simulation results show that: (1) the switching cells see the largest voltage drop, and (2) the neighboring cells on each side also experience voltage drop. The closer the neighboring cell is to the switching cell, the larger the voltage drop experienced by the neighboring cell, which is created by the switching cell. To perform this analysis, the power distribution network was extracted using a commercial tool and one cell was forced to switch at a time to measure voltage drop on each of the eight adjacent cells.

This analysis clearly demonstrates that the current induced by the switching of one cell has influence on the voltage drop of other cells connected to the same power rail. Thus, to maximize the voltage drop on one particular cell we can maximize the switching activity of the neighboring cells that are sharing the same power rail.

As shown in Figure 1, cell *G3* is in the critical path *PathX*. To maximize the effects of power supply noise on *G3*, transitions can be generated on other nearby cells whose current contributes to the voltage drop on cell *G3*. In this figure, cells directly adjacent to G3 and those that extend beyond the right and left of ViaA and ViaB, respectively, are classified as neighboring cells. The range beyond the right of ViaA and left of ViaB is determined by the amount of current drawn by cell G3. For example, the analysis shown in Figure 2, when cell 1 switches, the voltage drop experienced at cell 8 is almost negligible. Using such analysis, we define the neighborhood cell range. We will discuss the range of the neighboring cells we used in this work in Section III.

In this paper, we utilize this localized property of the voltage drop to maximize voltage drop on cells along the critical paths. The pattern generated by this method represents worst-case voltage drop for cells on critical paths and results in more accurate depiction of worse case timing performance.

B. Voltage Drop Effects on Path Delay

The IR-drop and ground bounce effects decrease the effective supply voltage of the gate under consideration, which will reduce its driving strength and thus increase the gate delay. Path delay consists of two parts: gate delays and interconnect delays. The increase in gate delays has direct impact on the path delay. To illustrate the relation between path delay and its associated voltage drop, we target a functionally testable critical path in b19 benchmark. A PDF pattern is generated for the targeted path; we fill the don't-care bits in the pattern randomly 1000 times to generate 1000 PDF patterns that test the same path. Figure 3 shows the delay of the path under test after each of the 1000 randomly-filled PDF patterns were applied, resulting in different voltage drops. The x-axis shows the average voltage drop across all the cells on the critical path. The correlation coefficient is 0.99 which shows a tight correlation between path delay and average voltage drop of the gates on this path. Similar analysis and results have been performed for more paths located in different locations on the layout and similar results have been observed.

III. Pattern Generation

After the physical design and parasitic information has been extracted, we identify critical paths using a commercial timing analysis tool. To maximize the power supply noise on each targeted path, one pattern for each path is generated. As shown

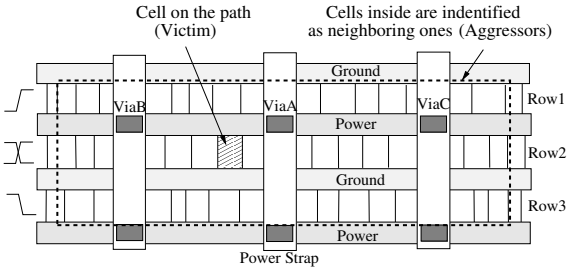

Fig. 5. Critical path cell (victim) and neighboring cell (aggressor) identification step of layout-aware pattern generation. Aggressors are targeted as fault sites to increase IR-drop/ground bounce for each cell in the critical path.

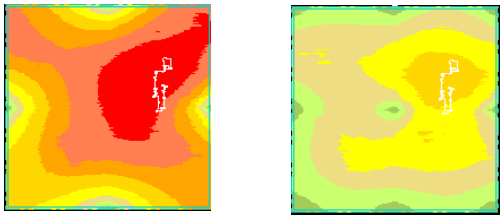

Fig. 6. IR-drop plot for path *P1* with pattern generated using our procedure in (a) wire-bond package (b) flip-chip package.

in Figure 4, the proposed pattern generation procedure consists of three major steps: 1) Cell identification; 2) Virtual test point insertion; and 3) Layout-aware TDF ATPG. Each of these steps are briefly described in the following.

A. Cell Identification

A DEF (Design Exchange Format) file is used to identify the cell location of the critical path in the layout. The DEF file contains the physical placement information of the elements in the circuit.

As discussed in Section II, to maximize voltage drop effects on each cell in the critical path, the goal is to generate transitions on the nearby cells which share the same power/ground rail. Therefore, for each cell on the path, we also identify cells that are within a pre-defined range and are connected to the same power/ground rail.

Figure 5 shows a cell on the critical path on which we intend to generate a high IR-drop/ground-bounce voltage. We refer to this as a "victim" cell. As seen in Figure 5, the victim cell is close to via *ViaA*. Based on our simulation results, the switching current from farther cells contributes less to the voltage drop of the victim cell. To increase the current flowing through the power rail and vias, we select cells around its two neighboring vias, *ViaB* and *ViaC*, to generate switching activity. We refer to these cells as "aggressors" because their switching activity can impact the voltage drop and the performance of the victim cell. Based on this criteria, we extract a gate list which contains all victim cells and aggressor cells for the targeted critical path.

B. Virtual Test Points Insertion

To generate patterns that increase the switching activity of cells on the gate list identified in Step 1, transition delay fault (TDF) ATPG is used to fill in don't-care bits in the target path's PDF pattern. However, for TDF ATPG, a transition fault will be considered detected only when it is activated at the fault site and propagated to an observation point. Since only the actual switching is necessary, propagating the transition to an observation point is unnecessary and may be creating additional care-bits that could be better used to activate a transition at another fault site. Also, the transition may only be activated but cannot be propagated. Thus, while the desired effect would be generated, the pattern would not be kept by the ATPG.

To avoid these issues, virtual test points are inserted at the output of these cells. Outputs of all identified gates are targeted fault sites. Existing the flip-flops in the design are considered as observation points during TDF pattern generation. The virtual test points provide new observation points to (i) reduce the amount of effort the ATPG needs to propagate the transition to an observation point; (ii) eliminate the effort needed by propagating the fault effect to a primary output or flip-flop; and (iii) increase the number of transitions. The effect of netlist alteration is only for TDF pattern generation and has *no effect* on the final design of the chip. The new netlist, called a temporary netlist, with virtual test points inserted is used during ATPG for pattern generation in our proposed procedure.

C. PDF-Constrained TDF ATPG

To ensure the critical path is tested during layout-aware delay test pattern generation, a PDF pattern is first generated and used to provide constraints during TDF pattern generation. We generate a robust PDF pattern while leaving all don't-care bits unfilled. To ensure the pattern is compatible with TDF pattern generation, the pattern is applied using an LOC clocking scheme. From the PDF pattern, any states filled with a care-bit are then extracted and utilized as a constraint during TDF pattern generation.

To generate switching activity that can increase IR-drop and ground bounce, we add slow-to-rise faults at aggressor cells that share the same power rail as the victim cell (Row 1 in Figure 5) and slow-to-fall faults at aggressor cells that share a common ground rail (Row 3 in Figure 5). As for cells in the same row (Row 2 in Figure 5) with the victim cell on the critical path, we add both slow-to-rise and slow-to-fall transition faults for both large IR-drop and ground-bounce voltage. This is used to generate the TDF fault list from the gate list identified in Step *1* for each victim cell. If more than one cell in a critical path are connected to the same power/ground rail, then the nearby cell (aggressor cell) region will be determined based on the proximity of the victim cells. If the victim cells are very close, then their nearby cell region may overlap, resulting in some shared aggressor cells. If they are far from each other while connected to the same power/ground rail, each victim cell will have a distinct set of aggressor cells.

TABLE I

VOLTAGE DROP (IR-DROP + GROUND BOUNCE) AND PATH DELAY ANALYSIS FOR LAYOUT-AWARE TDF PATTERN AND BEST RANDOM PATTERN IN *b19* BENCHMARK.

Path #	Wire-Bond				Flip-Chip			
	Average voltage drop (mv)		Path delay (ns)		Average voltage drop (mv)		Path delay (ns)	
	Random	Our Pattern	Random	Our Pattern	Random	Our Pattern	Random	Our Pattern
1	154.5	172.1	8.840	8.903	86.6	100.3	8.583	8.633
2	128.9	129.5	8.966	9.496	61.3	65.9	9.268	9.278
3	154.8	161.7	8.827	8.859	82.5	89.4	8.5621	8.574
4	151.0	156.2	8.744	8.769	72.4	75.4	8.474	8.481
5	111.1	119.4	8.586	8.613	41.9	60.9	8.402	8.422
6	102.9	109.8	8.582	8.597	52.9	56.2	8.408	8.419

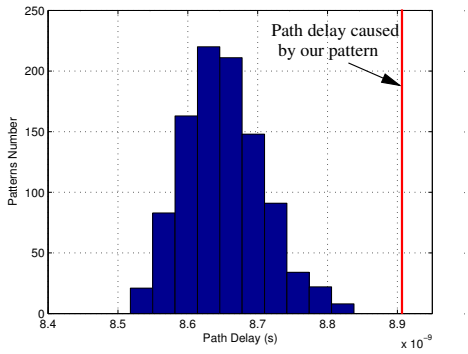

Fig. 7. Path delay distribution for path *P1* with 1000 random-filled PDF patterns and pattern generated by our proposed method in wire-bond package.

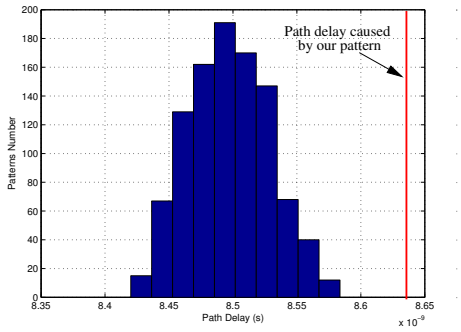

Fig. 8. Path delay distribution for path *P1* with 1000 random-filled PDF patterns and pattern generated by our proposed method in flip-chip package.

IV. EXPERIMENTAL RESULTS

We implemented layout-aware pattern generation on ITC'99 benchmark *b19*, which has 190,213 gates and 6642 flip-flops. The physical layout was designed using the 180nm Cadence Generic Standard Cell Library [10] with 1.8 V as its typical supply voltage. Critical paths were identified with a commercial static timing analysis tool. The program for parsing the DEF file to extract the victim and aggressor cell list was developed in C. To validate the patterns, we performed power/ground rail analysis using a commercial tool using the pattern generated by our proposed method. Then, the instance power/ground voltage profiles were extracted with a Perl script

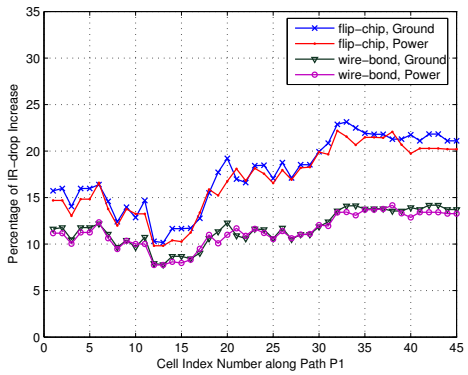

Fig. 9. Percentage of IR-drop increase (our pattern vs. best random pattern) on Power and Ground pins of cells along path *P1* in wire-bond and flip-chip packages;

and applied to the SPICE netlist. SPICE simulation of the critical path using the extracted instance supply voltages were used to analyze the path delay.

Figure 6 presents the b19 IR-drop plots of a pattern generated with our proposed method targeting critical path *P1*. IR-drop plots for both wire-bond and flip-chip packaging styles are shown in this figure. The darkest region in Figure 6(a) represents regions with IR-drop voltage over 80 *mV*. The effective voltage drop (IR-drop + ground bounce) for cells in the same region is above 160 *mV*, which is about 9% of the ideal supply voltage. Path *P1* has been highlighted in the IR-drop plots to show the effectiveness of targeted switching around Path P1. There were four pairs of power/ground pads in the wire-bond chip, which were placed in the middle of each side of the chip.

The flip-chip, shown in Figure 6(b), uses nine C4 bumps distributed across the chip. The IR-drop observed for cells around the path in flip-chip is above 40 *mV*. The effective voltage drop is around 100 *mV* for cells around path *P1*. To verify the effectiveness of our proposed pattern generation method, we compared its path delay performance with 1000 random patterns. The random PDF patterns were generated as follows: first, a single PDF pattern was generated targeting path *P1* with don't-care bits unfilled, then 1000 PDF patterns were generated by filling the don't-care bits randomly 1000 times. We ran the pattern validation process for our pattern

TABLE II
CELL NUMBERS AND CPU RUN TIME FOR PATHS IN *b19* BENCHMARK.

Path #	Number of Cells on Path	CPU Run Time	
		Random Pattern	Our Pattern
1	45	49*hrs*	605*s*
2	45	50*hrs*	612*s*
3	45	49*hrs*	600*s*
4	43	48*hrs*	580*s*
5	42	49*hrs*	568*s*
6	42	50*hrs*	570*s*

and the random-filled patterns to measure their path delays. Figures 7 and 8 illustrate the results for the delay for wire-bond and flip-chip packing styles, respectively. As seen from both results, the path delays caused by patterns generated from our proposed method are longer than that of any random patterns.

To further verify the effectiveness of our proposed method on maximizing the supply noise around the critical path, we compared the effective IR-drop voltages of cells in the critical path when applying our pattern and when applying the *best* (highest delay) pattern of the 1000 random patterns. Figure 9 shows the percentage of IR-drop increase on the power and ground pins for each cell in the critical path *P1*. Results for both wire-bond and flip-chip packages are presented. For the wire-bond design, our pattern can induce an 11% greater voltage drop than the best random pattern does, while for flip-chip design, a 17% greater voltage drop on cells in the critical path can be seen when comparing our pattern with the best random one.

Table I shows the results for 6 critical paths of b19. The results for the best random pattern and the pattern generated by our proposed method are shown. The average effective voltage drop for the best random pattern and pattern generated by the proposed method is shown in columns 2–3 for wire bond and 6–7 for flip-chip. The respective total path delay are shown in columns 4–5 and columns 8–9. For path *P1*, the path delay for circuit with ideal power and ground supply voltage is 8.422 *ns*. Our pattern increases path delay by 0.481 *ns* which is 15% higher than that increased by the best random pattern in wire-bond chip. In flip-chip our pattern increases path delay 31% higher than that increased by the best random pattern.

The average effective voltage drop reported is the calculated average effective voltage drop across all cells in the critical path. Comparing the results obtained both for average effective voltage drop and path delay, we can see our pattern induces larger power supply noise and longer path delay than the best random pattern for all the targeted critical paths.

These experimental results clearly validate our proposed method and prove the effectiveness of our generated pattern. Generating a pattern using our method requires considerably less CPU run time than finding the a random pattern that may provide the longest path delay after simulating a large number (1000) of random patterns. Table II shows the cell counts of each targeted path and the CPU run time required by the two methods. The results show that our proposed method can generate one pattern in several minutes for a critical path which is much faster than running SPICE simulation for 1000 random patterns and selecting the one with the longest delay, which may require days of simulation.

Since we implemented our method on b19, a fair comparison with previously proposed methods [6] [7] [8] cannot be made since those results were on different benchmarks. However, since our proposed method is not iterative, it is significantly faster than previous approaches. Another important distinction is that our proposed method uses actual physical design information in addition to localized switching impact rather than only targeting increase in global switching activity.

V. CONCLUSION

In this paper, we have presented a novel layout-aware pattern generation procedure for testing critical paths under maximum power supply noise. The localized IR-drop and ground-bounce and their impact on path delay have been analyzed. To maximize the IR-drop/ground-bounce voltage on cells along critical paths, for each cell on the path, we selected cells in close proximity and generated switching activity using these identified aggressor cells. By increasing the switching activity around each cell in the critical path, the pattern generated by our method effectively increases the IR-drop and ground bounce along that path. The experimental results for several paths show that the layout-aware TDF ATPG is able to increase the path delay significantly for both wire-bond and flip chips, and is considerably faster when compared to selecting a random pattern with the worst voltage drop effects from a large set of random patterns. The pattern generated by our proposed method can provide a realistic estimation of worst-case delay for the critical paths.

REFERENCES

[1] A. H. Ajami, K. Banerjee, A. Mehrotra, and M. Pedram, "Analysis of IR-Drop Scaling with Implications for Deep Submicron P/G Network Designs" in Proc. of the *Fourth International Symposium on Quality Electronic Design (ISQED'03)*, 2003, pp. 35-40

[2] R. Saleh, S. Z. Hussain, S. Rochel, and D. Overhauser, "Clock skew verification in the presence of IR-Drop in the power distribution network," in *IEEE Trans. on Computer-Aided Design*, vol. 19, No. 6, 2000, pp.635-644

[3] S. Pant, D. Blaauw, V. Zolotov, S. Sundareswaran, and R. Panda, "Vectorless Analysis of Supply Noise Induced Delay Variation," in Proc. of the *2003 IEEE/ACM International Conference on Computer-Aided Design*, 2003, pp 184-191

[4] C. Tirumurti, S. Kundu, S. K. Susmita, and Y. S. Change "A Modeling Approach for Addressing Power Supply Switching Noise Related Failures of Integrated Circuits," in Proc. of the *Design, Automation and Test in Europe Conference*, 2004, pp. 1078-1083

[5] J. Wang, D. M. Walker, X. Lu, A. Majhi, B. Kruseman, G. Gronthoud, L. E. Villagra, P. J. A. M. van de Wiel, and S. Eichenberger, " Modeling power supply noise in delay testing," in *IEEE Design & Test*, vol. 24, issue 3, 2007, pp. 226-234

[6] M. Nourani, M. Tehranipoor, and N. Ahmed, "Pattern Generation and Estimation for Power Supply Noise Analysis," in Proc. of the *23rd IEEE VLSI Test Symposium*, 2005, pp. 439-444

[7] J. J. Liou, A. Krstic, Y. M. Jiang, and K. T. Cheng, "Path Selection and Pattern Generation for Dynamic Timing Analysis Considering Power Supply Noise Effects," in Proc. of the *2000 IEEE/ACM international conference on Computer-aided design*, 2000, pp. 493-497

[8] A. Krstic, Y. M. Jiang, K. T. Cheng, "Pattern Generation for Delay Testing and Dynmaic Timing analysis Considering Power-Supply Noise Effects," *IEEE Transactions on CAD*, vol. 20, No. 3, pp. 416-425, 2001

[9] S. Zhao and K. Roy, "Estimation of Switching Noise on Power Supply Lines in Deep Sub-micro CMOS circuits," in Proc. *Thirteenth Int. Conf. on VLSI Design*, pp. 168-173, 2000

[10] http://crete.cadence.com, 0.18um standard cell GSCLib library version 2.0, Cadence, Inc., 2005