Supply Voltage Noise Aware ATPG for Transition Delay Faults *

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ABSTRACT

The sensitivity of very deep submicron designs to supply voltage noise is increasing due to higher path delay variations and reduced noise margins with supply noise scaling. The supply noise of delay test during at-speed launch and capture is significantly larger compared to normal circuit operation since larger number of transitions occur within a short time frame. Our simulations have shown that for identical switching activity, a pattern with a short switching time frame window will surge more current from the power network, thereby causing higher IR-drop. In this paper, we propose a novel method to measure the average power of at-speed test patterns, referred to as switching cycle average power (SCAP). We present a case study of the IR-drop effects on design performance during at-speed test. A new practical framework is proposed to generate supply noise tolerant delay test patterns. The proposed framework uses existing commercial ATPG tools and a wrapper is added around them. The results demonstrate that the new patterns generated using our framework will significantly reduce the supply noise.

I. INTRODUCTION

As technology shrinks and functional density and frequency increase, test engineers face more challenging problems to deal with. One important issue of testing today's nanometer, high-speed designs is the increasing number of timing-related defects. Transition and path delay fault models are increasingly used to target such defects. Among these two, the transition fault model is widely practiced in industry to test delay-induced defects and is considered a cost-effective alternative to functional pattern generation [1][2]. A pattern pair is generated to initialize the target node and launch a transition using two fast clock cycles (rated clock frequency). The at-speed launch and capture in addition to large number of switching in the circuit can cause excessive peak power and result in large IR-drop.

Supply noise (including IR-drop, ground bounce, and Ldi/dt) effects have become more significant in recent years and need to be efficiently taken into consideration, as they pose design, test and reliability challenges for the chip manufacturers/foundries. This situation has grown more complicated with reducing supply voltage and the limitation of further reduction of threshold voltage. The reduced voltage difference between the VDD and VSS pins of a standard cell will reduce the cells operating performance and may result in chip performance reduction if the cell is on a critical path. The IR-drop also reduces the cells noise immunity and in some cases may lead to functional failures [3].

There is a growing concern in EDA and semiconductor industry for supply voltage noise and timing aware ATPGs. In order to simplify the pattern generation process, traditionally ATPGs consider zero delay gate model and target as many faults with one pattern as possible. In other words, operating and manufacturing conditions are ignored during ATPG. Patterns generated using such ATPGs may cause large number of transitions in the circuit which may not occur during functional operating condition. As a result, a design that may *not* have a delay fault may fail a delay test pattern due to excessive IR-drop related effects. This causes overkill and needs to be carefully addressed when testing today's large high-speed designs. Therefore, new pattern generation methods must be proposed to generate test patterns that reliably distinguish between good and bad chips.

Supply voltage noise would be even more problematic during faster-than-at-speed test where the test patterns are applied at higher than functional frequencies. Faster-than-at-speed test methods have been proposed to detect small delay defects by increasing the test frequency, i.e. reducing the positive slack of the path [4]. This however may result in false identification of good chips to be faulty due to supply noise rather than small delay defects [5].

A. Related Prior Work

Three major scan-based techniques have been proposed for transition delay fault test, i.e. launch-off-shift [6], launch-off-capture [7], and enhanced scan [8]. In all three methods, a pattern pair (V1, V2) is applied to target delay faults but with different launch mechanisms. Pattern V2 for launch-off-shift, launch-off-capture, and enhanced scan is generated using last shift, functional response, and arbitrary using ATPG, respectively. Various techniques have also been proposed to improve the quality of at-speed test by increasing fault coverage and reducing pattern count [9], avoiding functionally untestable faults [10], or reducing scan enable design effort [11]. Techniques have been proposed to detect small delay defects either by improving existing ATPGs [12] or using faster-than-at-speed test application [4]. Note that in all cases, the launch pattern and capture clock must be applied at either rated clock frequency for traditional at-speed test or higher than clock frequency for faster-than-at-speed test. Both increase the IR-drop and may degrade the design performance.

Authors in [13] address the issue of overkill during delay test and propose a vector-based approach for power supply noise analysis in test compaction. A power supply noise model is developed and used during test compaction. The procedure may

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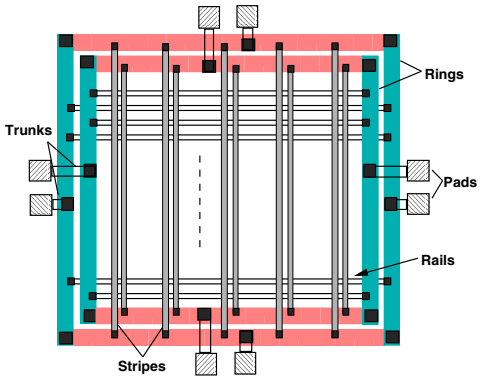

Fig. 1. Power/Ground Distribution Network.

become slow for large designs since all the patterns are generated without *random-fill* and the power supply noise needs to be estimated in every compaction loop. The method proposed in [14] verifies test vectors for IR-drop failures and identifies failing vectors. The method estimates the average current drawn from power rails and compares it against a pre-defined threshold set by designer. A pattern generation technique is proposed in [15] by building current/voltage libraries to maximize the power supply noise along targeted paths and cause longer propagation delays for the nodes along the paths. The computation complexity of the pattern generation procedure is high since it targets one pattern at a time.

B. Contribution and Paper Organization

In this paper, a new method is presented to measure the average power during at-speed test patterns (during fast launch and capture of at-speed test), referred to as *switching cycle average power*. The method considers both the length of the paths affected by each pattern and switching occurred during that time frame window as opposed to calculating switching power for entire clock cycle in statistical approach. A novel pattern generation procedure taking supply voltage noise into account is proposed ensuring that the supply noise will always be lower than defined noise threshold. The proposed procedure uses existing commercial ATPG tools and adds wrapper around them. The results show that the new pattern set generated using pur proposed procedure significantly reduce the IR-drop.

The rest of the paper is organized as follows. Section II explains a case study with detailed statistical and dynamic IR-drop analysis for at-speed test pattern application. Section III presents a new power model to measure the average switching power for at-speed patterns. The framework with pattern generation and a technique to measure the switching cycle average power is discussed in Section IV. The experimental results are presented in Section V. Finally, concluding remarks are in Section VI.

II. Case Study

In this section, firstly we describe the physical design implementation and statistical IR-drop analysis. We, then present a detailed dynamic IR-drop analysis for two types of patterns with different path delay distribution. Also, a new power model is explained to measure the average power of at-speed test patterns which takes both the switching activity and the pattern path delay distribution into account.

A. Physical Design Implementation

For our experimentation, we had selected an ITC'99 benchmark design $b19$ and the physical design implementation was performed using Cadence SOC Encounter place and route tool [16]. The design contains almost 219K gates, 51 IO pads, and about 6,642 flip-flops. Scan-based test insertion was performed using Synopsys DFT Compiler [17] with eight scan chains and a slow speed scan enable is used for launch-off-capture transition fault test. During physical design, the design is timing closed for an operating frequency of 142MHz at nominal operating voltage ($1.8V$) and temperature (25^oC) conditions. A slow scan shift speed of 10MHz was used. It is implemented in $180nm$ standard cell library [18]. Note that at this point of experiments, no decoupling capacitances were inserted.

The power-planning for the design was performed assuming a net toggle probability of 20% during functional operation. Figure 1 shows the power/ground distribution network of the chip. Power rings ($width = 20\mu m$) were created using higher-level routing layers (Metal5 and Metal6) and carry power around the standard cell core area. Four power (VDD) and ground (VSS) pads each were inserted and connected to the respective rings with wires referred to as trunks. After creating the power rings, power and ground is routed to the standard cells using stripes and rails. The stripes ($width = 10\mu m$) were created using routing layer Metal4 and a distance of $100\mu m$ between adjacent stripes connecting power rings. The design was then placed and routed along with clock-tree synthesis and scan cell ordering to minimize scan chain wirelength.

B. Statistical IR-drop Analysis

In order to determine an estimate of functional IR-drop, the design net parasitics (resistance and capacitance) were extracted using Synopsys STAR-RCXT [17] extraction tool. The average statistical IR-drop using vector-less approach was measured for both VDD and VSS nets considering 20% net toggle probability during functional operation. The results showed 2.8% voltage drop in VDD and a voltage bounce of 4.5% for the VSS net, which can be considered negligible. However, such an analysis provides an underestimation of both average and peak IR-drop even during functional operation. This is because the tool considers the probability of net toggle activity over the entire cycle period (vector-less approach). However, to measure IR-drop more accurately during test a vector-based IR-drop method must be devised to consider both the average time frame window for each pattern during which the entire switching occurs and the simultaneous switching.

To measure the average IR-drop experienced by the transitions, it is important to estimate the average switching time frame. The time span during which all the transitions occur is referred to as the *switching time frame window (STW)*. For a transition fault pattern, the maximum path length affected determines this time frame. Note that for different test vectors, the longest path exercised will be different. From our previous experiments on the same design during transition fault test patterns [19], we have seen an *average switching time frame window* close to half the clock cycle period which is mainly because the ATPG tools tend to detect delay faults through short paths. This shows that the actual average functional power

TABLE I

STATISTICAL FUNCTIONAL IR-DROP ANALYSIS RESULTS FOR ITC'99 BENCHMARK (*b19*).

	Avg. Switching Power [mW]	*Avg. IR-drop [V]*	
		VDD	VSS
Case1 (Full cycle period)	96.3	0.05	0.084
Case2 (Half cycle period)	190.6	0.11	0.162

surge observed during an average switching time frame for a pattern is almost twice of the measured value during one cycle period. This observation shows that if N flip-flops or nets toggle during one capture event, the same N flip-flops will toggle irrespective of the frequency. The effect on IR-drop will now be more pronounced if the toggle happens in a smaller window, thus tying IR-drop effects to the path delays affected by test patterns.

Table I shows the statistically measured average power consumption for the entire cycle period *(Case1)* and average switching time frame *(Case2)* for half cycle period. It also shows the average IR-drop reported for the two cases measured using Cadence SOC Encounter tool. It can be noticed that the average IR-drop is almost doubled when the switching time frame window is reduced to half of the cycle period. Although, this might appear over pessimistic but it provides a good estimate of the IR-drop which the design will experience during functional operation. Also, *Case2* provides an average *power threshold* that can be used to identify high toggle activity transition fault test patterns at a later stage.

C. Dynamic IR-drop Analysis

The actual IR-drop during transition fault test patterns is much higher compared to statistical IR-drop due to very high switching activity and smaller switching time frame. In this section, we analyze the IR-drop effects of two types of transition fault test patterns (*P1 and P2*) with almost the same switching activity but with different switching time frame windows. The maximum path delay for patterns *P1* and *P2* are $t_{d(P_1)} = 4854ps$ and $t_{d(P_2)} = 2313ps$, respectively and the clock period being $T = 7000ps$. This implies that pattern *P2* exercises more number of short paths (that is, larger number of simultaneous switching) which increases the probability of higher IR-drop.

Figure 2 shows the clock timing waveform used for dynamic IR-drop analysis. The clock insertion delay is the time taken by the clock signal from the chip periphery to all the registers in the design and it is represented as t_i. For clarification, we have not shown clock edge uncertainty which is also included in t_i. The entire clock network switching activity for each clock edge occurs in this time frame. Since, the clock switching power forms a major component in the total power drawn, it is also included in our power measurement. If the switching time frame window is slightly less than half the cycle period (see $t_{d(P_2)}$ in Figure 2), the negative clock edge switching activity is also considered. This is reasonable as the clock network already starts to switch close to the end of the switching window ($t_{d(P_2)}$), assuming clock uncertainty and process variations. In general, the switching time frame window for dynamic IR-drop analysis is measured using the following formulation:

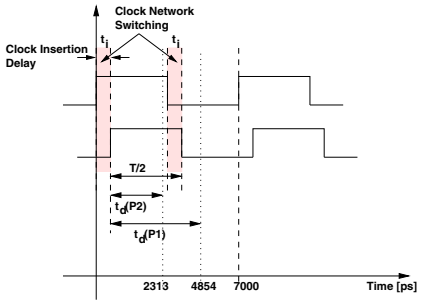

Fig. 2. Clock timing waveform used for dynamic IR-drop analysis.

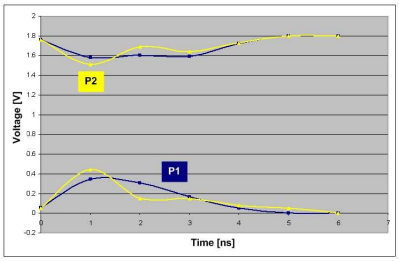

Fig. 3. IR-drop effects on VDD and VSS during pattern *P1* and *P2* application within 7 *ns* caputre window.

$$STW_i = \begin{cases} t_i + T/2 & \text{if } t_{d(P_i)} \leq T/2 \\ t_i + t_{d(P_i)} & \text{if } t_{d(P_i)} > T/2 \end{cases}$$

To measure the IR-drop of the pattern, the switching activity inside the circuit was captured in the standard value change dump (VCD) format during gate-level timing simulation. The timing information of the gates and the extracted parasitic interconnect delay information was back-annotated using the standard delay format (SDF) file. The switching activity information (VCD file) along with physical design and technology library information is used by SOC Encounter tool [16] to estimate the dynamic IR-drop of the pattern. Figure 3 shows the VDD (VSS) voltage waveforms during the at-speed launch and capture cycles for pattern *P1* and *P2*. To measure the IR-drop, the launch-to-capture window $(7ns) + t_i$ was split into $1ns$ time frames and average IR-drop was measured in each time frame. It can be noticed that the effect of IR-drop is maximum in the beginning of the clock cycle due to high simultaneous switching activity and gradually decreases. Also, the effect of IR-drop is maximum in pattern *P2* as high switching activity occurs in a smaller switching time frame window.

Figures 4 and 5 show the average IR-drop plots on the ground (VSS) network for patterns *P1* and *P2* during their respective switching time frame windows. The IR-drop plots were obtained from the Cadence SOC Encounter tool [16] measured across the respective switching time frame for each pattern. Note that, for pattern P2, the IR-drop in a large portion of the chip increases which results in reduced effective voltage difference between the VDD and VSS ports observed by each gate in that region. This might result in higher performance degradation or functional failure of the circuit due to excessive noise.

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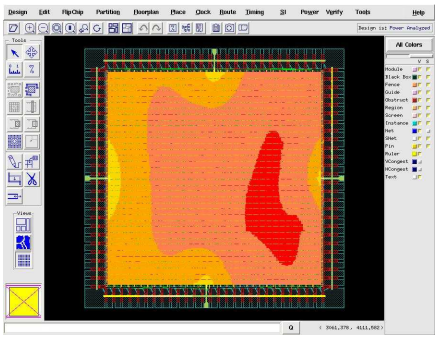

Fig. 4. IR-drop plot in VSS net for pattern *P1*.

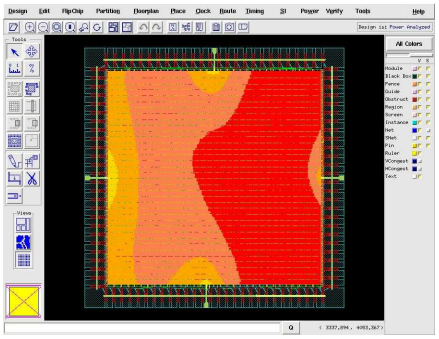

Fig. 5. IR-drop plot in VSS net for pattern *P2*.

III. Average Power Model

As we explained in the previous sections, the IR-drop depends on the total switching capacitance and the time frame window during which it occurs. Since, dynamic IR-drop analysis for each delay test pattern is prohibitively expensive, we require a model to identify test patterns which have a high probability of failure due to IR-drop effects, during their application. The *cycle average power (CAP)* [20] is defined as the average power consumed during a single tester cycle. However, it does not factor in the varying time frame window of the entire switching activity for each pattern. Therefore, a pattern with relatively lesser switching activity but with a very short switching time frame window will not be considered as a potential pattern of IR-drop failure by the CAP power model. Therefore, we define a new term referred to as *switching cycle average power (SCAP)* which is the average power consumed by the test pattern during the time frame of the entire switching activity (STW). CAP and SCAP are calculated by:

$$CAP = (\Sigma C_i \times VDD^2)/T$$

$$SCAP = (\Sigma C_i \times VDD^2)/STW$$

where C_i is the output gate capacitance of gate G_i. Table II shows the comparison of average power and IR-drop analysis of pattern *P2* using the CAP and SCAP model. It can be noticed that the power surge during the switching time frame window (SCAP) is $1.3X$ higher compared to the cycle average power. Also, the average IR-drop using CAP model ($0.16V$) reported is within the V_{min} operating conditions for which the IR-drop effect will not be of concern. In general, during sign-off, the design is made sure to work under V_{min} and V_{max} operating conditions. However, with the SCAP model, the average IR-drop experience by the design on VSS network ($0.216V$) during the switching interval exceeds it by 34 %.

TABLE II

Average dynamic power/IR-drop analysis results of a pattern for CAP and SCAP model.

	Avg. Switching Power [mW]	*Avg. IR-drop [V]*	
		VDD	VSS
CAP	163	0.120	0.161
SCAP	211	0.136	0.216

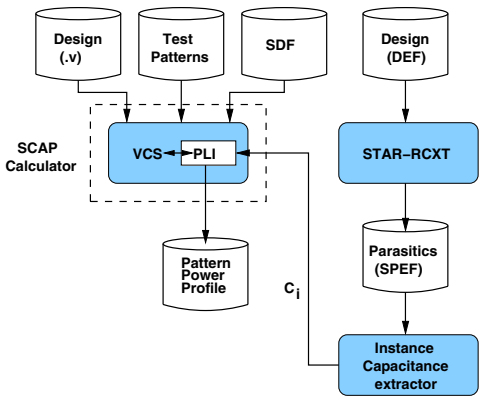

Fig. 6. SCAP calculator using Synopsys VCS simulator.

IV. Pattern Generation Framework

As explained in Section II, the switching cycle average power provides a more practical measure to identify patterns with very high IR-drop effects bypassing the expensive dynamic IR-drop analysis per pattern. Since, the transition fault pattern set has varying path delays and switching activity, the pattern generation problem can be divided into two sub-problems: *A*) to measure the switching cycle average power (SCAP) for each pattern and *B*) to generate a new pattern set ensuring that the IR-drop will remain under a pre-defined threshold. Both will be discussed in the following sub-sections.

A. SCAP Calculator

To determine the SCAP of each pattern in the transition fault pattern set, we need the following information: 1) the gates switching inside the circuit, 2) output capacitance of each gate and 3) the switching time frame window. Simulation-based techniques can be used to capture the switching activity information in the standard *value change dump (VCD)* format. But, this technique is sufficient only to analyze a very small number of patterns due to the extremely large size of VCD files for large designs.

To overcome this problem, we use programming language interface (PLI) routines during gate-level verilog simulation. The PLI provides a standard interface to the internal data representation of the design during simulation. Figure 6 shows the SCAP calculation flow. The capacitance per each gate instance

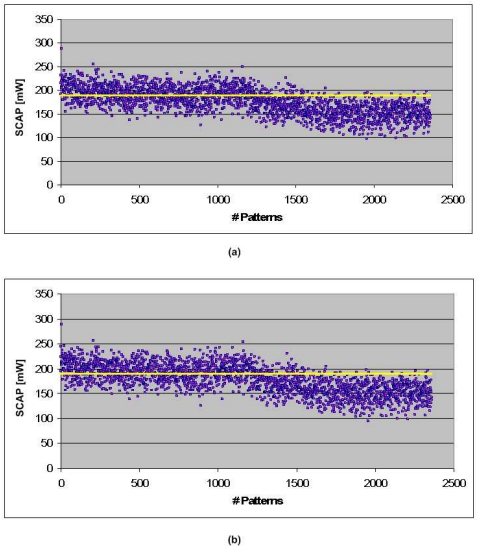

Fig. 7. Switching cycle average power (SCAP) measured for each transition fault test pattern (a) VDD network and (b) VSS network.

is extracted from the RC parasitics file (*Standard parasitics exchange format (SPEF)*) generated using Synopsys STAR-RCXT extraction tool. We have developed a PLI which can be plugged into Synopsys VCS gate level simulator which acts as SCAP calculator during simulation. It reports the SCAP value for VDD and VSS power network for each pattern during the launch-to-capture window in the launch-off-capture transition fault pattern set. The above procedure using PLI interface avoids the VCD file generation for estimation of switching power.

Figure 7 shows the SCAP value for VDD and VSS network in each transition fault test pattern during the launch and capture functional cycles of the launch-off-capture pattern. It can be noticed that the initial patterns have higher switching cycle average power and then very gradually reduces. This is because the initial patterns detect most of the transition faults (exercise more paths) and the later patterns target the hard-to-detect faults.

B. Pattern Generation

In the first phase, the launch-off-capture transition fault pattern set (2630 patterns) were generated using Synopsys TetraMax [17] in the conventional manner with random fill of don't-care bits during ATPG. Figure 8 shows the new pattern generation framework which uses existing commercial ATPG tools. The generated patterns are simulated using a gate-level simulator and the SCAP value for each pattern is measured as explained in Section IV-A. After obtaining the power pattern profile, it is important to set a threshold to shortlist the patterns with very high SCAP value which relates to a lower tolerance to IR-drop effects. For this, we use the average functional switching power estimated using statistical-based approach as explained in Section II-B for the SCAP threshold ans shown in Table I. A 20% toggle activity over an average switching time frame of half the clock cycle period is assumed. This number is usually defined by designer during power network synthesis. The remaining patterns are called *IR-drop tolerant patterns*.

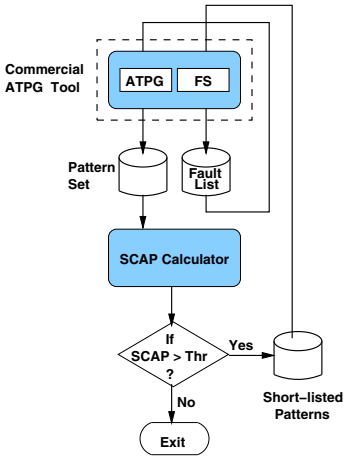

Fig. 8. New pattern generation framework.

Based on the functional operation SCAP threshold for both the VDD and VSS network, the short-listed patterns are fault simulated using the Synopsys TetraMax tool to obtain the list of extra faults detected on top of the remaining IR-drop tolerant patterns. In the next phase of pattern generation, new patterns are generated for these set of faults with *adjacent-fill* or *fill-X* ($X = 0$ or 1) options. Adjacent fill causes don't-care scan cells to be filled with the value of the first downstream scan cell with a defined/care value (i.e. it creates runs of 0's and 1's in the test pattern). This option in the ATPG tool is useful to minimize power usage as it significantly increases the correlation between the initialization and launch patterns. Although, this reduced signal switching comes at the expense of slightly higher pattern count.

V. Experimental Results

We had generated launch-off-capture transition fault test patterns (2360 patterns) using conventional random fill method. As shown in Figure 7, the SCAP threshold was set to 190.6*mW* based on the measured value in Table I for 20% toggle activity during functional operation for a switching time frame window of half the clock cycle. Based on this threshold, approximately 860 patterns were short listed with high SCAP value compared to the threshold. In the new ATPG, first the IR-drop tolerant patterns are fault simulated. Then the short listed patterns are fault simulated and it was observed that they contribute almost 10% of test coverage to the total coverage over the IR-drop tolerant test patterns.

In the next step, we generated patterns using the don't-care fill options built in Synopsys TetraMax for low power patterns. Note that other previously proposed low power pattern generation techniques could also be used. We generated patterns with three different fill options: *Case1: fill-0*, causes all don't-care scan cells to be filled with 0's, *Case2: fill-1*, causes all don't-care scan cells to be filled with 1's and *Case3: fill-adjacent*, causes don't-care scan cells to be filled with the value of the first adjacent scan cell with a defined/care value. *Case3* is mostly useful to minimize power usage during scan shifting by reducing signal switching at the expense of higher pattern count. However, in our experiments we are trying to reduce the

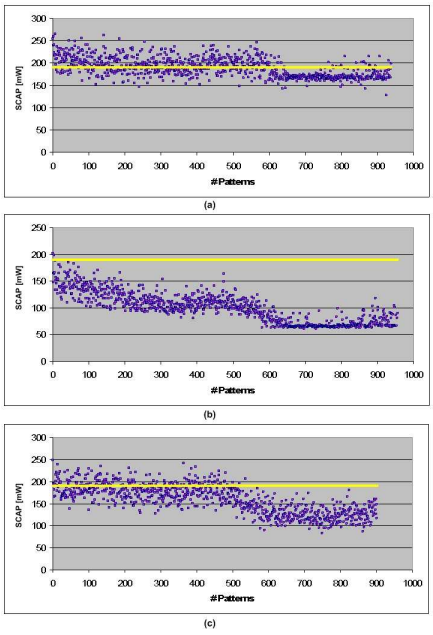

Fig. 9. Switching cycle average power (SCAP) in VDD network for the low switching activity test patterns generated in three cases: (a) *fill-1*, (b) *fill-0* and (c) *fill-adjacent*

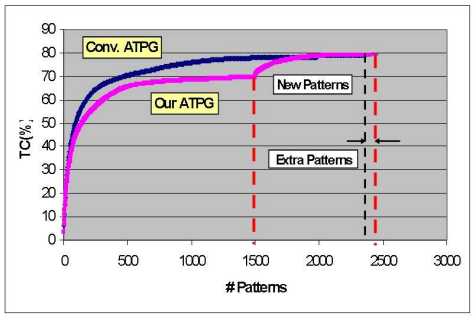

Fig. 10. Test coverage curves for conventional ATPG and our new supply aware ATPG.

switching activity between the launch and capture window of the launch-off-capture patterns.

Figure 9 shows the switching cycle average power for the additional patterns generated in the three different cases. The number of patterns generated were 939, 957 and 900 in *Case1*, *Case2* and *Case3*, respectively. It can be noticed that *fill-0* provided the best results with almost all the patterns below the threshold. Figure 10 shows the test coverage curve for the two pattern generation methods. It can be seen that our technique generates approximately 957 patterns (*fill-0*) for the 10% coverage of the short-listed patterns, which is a very slight increase in the number of patterns (approximately 97 additional patterns). Therefore, the increase in test time is not very significant with almost all of the patterns in the new pattern set within the threshold limit.

VI. Conclusion

We have presented a detailed analysis of at-speed techniques which illustrates that modeling IR-drop requires both the switching activity and the switching time frame window, i.e. the path delay distribution of the pattern. The switching cycle average power (SCAP) proposed captures both of these effects and provides a good model to identify patterns with higher IR-drop effects. We have proposed a new framework for generating transition fault test patterns which are tolerant to IR-drop effects. This avoids the false classification of good die as faulty, where the fault effects are caused due to IR drop related reasons. The experimental results show approximately 4 % increase in number of test patterns over the conventionally generated transition fault pattern set.

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