Radic: A Standard-Cell-Based Sensor for On-Chip Aging and Flip-Flop Metastability Measurements

Xiaoxiao Wang[1], Dat Tran[1], Saji George[1], LeRoy Winemberg[1], Nisar Ahmed[1],
Steve Palosh[1], Allan Dobin[1], and Mohammad Tehranipoor[2]
[1]Freescale Semiconductor, {xiaoxiao.wang, dat.tran, Saji.George, leroyw, nisar.ahmed,
steve.palosh, dobbin.allan}@freescale.com
[2]ECE Department, University of Connecticut, {tehrani}@engr.uconn.edu

Abstract

As process technology further scales, aging, noise and variations in integrated circuits (ICs) and systems become a major challenge to both the semiconductor and EDA industries, since a significantly increased mismatch is emerging between modeled and actual silicon behavior. Therefore, the addition of accurate and low-cost on-chip sensors is of great value to reduce the mismatch. This paper presents a standard-cell-based, novel, and accurate sensor for reliability analysis of digital ICs (Radic), in order to better understand the characteristics of gate/path aging and process variations' impact on timing performance. The Radic sensor performs aging, flip-flop (FF) metastability window and variation measurements on-chip. This sensor has been fabricated in a floating gate Freescale SOC in very advanced technology. The measurement results demonstrate that the resolution is better than 0.1ps, and the accuracy is kept throughout aging/process variation. Furthermore, reliability and FF metastability measurements are performed using the proposed sensor. The measurement results agree with the existing models.

Keywords: Frequency/delay Sensor, Aging Sensor, Metastability Window Measurement, NBTI, HCI, On-Chip Structure

1 Introduction

With gate lengths and oxide thicknesses shrinking, reliability and process variations have created a non-negligible gap between CMOS model and silicon performance. Several aging mechanisms can greatly affect reliability during the lifetime of a chip. These mechanisms include bias temperature instability (BTI), hot carrier injection (HCI), and oxide breakdown. Among the BTIs, as interface traps are more often to happen in PMOS transistors, negative bias temperature instability (NBTI) affecting PMOS is a more dominating aging effect compared to positive bias temperature instability (PBTI) affecting NMOS [1]. Both NBTI and PBTI increase the threshold voltage and degrade the speed of CMOS transistors. A comprehensive background and recent discoveries about NBTI effects can be found in [2]. The second significant aging effect is HCI [3], which is caused by the carriers in transistor channel being injected and trapped in the oxide by the electrical field either between gate and drain or substrate and gate, or by band-to-band tunneling for more advanced technologies [4]. Similar to NBTI, HCI also increases CMOS transistors' threshold voltage, however, the difference is that NMOS is more vulnerable to HCI [5]. Besides the reliability concerns, nowadays, process variations can generate 10% or more performance deviation among the gates of the same die [6]. The sequential instance's metastability window, which affects the setup and hold time, has been found to be very sensitive to process variations and critical to timing performance. The mechanism of FF metastability is presented in [7].

1.1 Previous Works

Works have been presented for aging characterization in literatures. I_{DDQ} measurement is used in [8] to characterize NBTI degradation. With NBTI induced threshold voltage increase, a reduction will be experienced in I_{DDQ} current of the circuit. Transistor-level NBTI measurement developed in [9] measures the transistor gate voltage (V_g) needed to turn on a transistor. Due to aging-induced threshold voltage increase, larger V_g is needed to turn on the transistor. However, this method, as well as the I_{DDQ}-based method, both need off-chip equipment to measure either currents or input voltage levels, which greatly increase test cost and limit their applications in large volume production test.

Architectures presented in [10] [11] [12] [13] [14] [15] [16] [17] measure the delay/degradation of a path/instance by on-chip architectures. [18] translates PMOS' saturation current reduction due to aging into the oscillation frequency degradation. However, these on-chip sensors contain analog or custom gates, which will throw a burden to structural test the defects inside them, since commercial design for test (DFT) and automatic test pattern generation (ATPG) tools cannot generate test points and patterns automatically. Furthermore, digital/analog boundaries are needed to separate some of the sensors from the digital sea of gate during pattern generation. For chips fabricated in large volume, a small individual-die test cost increase usually relates to a significant increase of production cost.

On-chip FF metastability window measurement architectures are presented in [7] [19] [20] [21]. However, off-

978-1-4673-1595-1/12/$31.00

chip signal generators and oscilloscopes are also required by all these techniques.

To reduce sensor manufacture/test cost and maximize accuracy, on-chip measurement architectures should be (i) of low design cost, (ii) of low test cost, (iii) robust against process variation/aging, and (iii) able to very accurately measure path delay and gate delay in order to perform silicon-to-model mismatch analysis.

1.2 Contributions

In this paper, we propose a standard cell based aging/metastability measurement architecture called Radic. This architecture provides the following advantages:

- It is composed of frequently used standard cells, hence it can be fully structural tested.
- It asks for no extra constraints in design stage.
- It is robust against variations and aging.
- It can accurately measure oscillator's frequency and FF's metastability window.

The proposed sensor has been recently successfully implemented on a Freescale SOC design with very advanced technology. The accuracy of the proposed architecture has been verified thoroughly by silicon experiments across Freescale die matrix.

This paper is organized as follows. In Section II, the architecture of Radic sensor will be presented. The accuracy and aging robustness of the proposed architecture are analyzed in Section III. In Section IV, the application-orientated measurement results are provided, and concluding remarks are presented in Section V.

2 The Architecture of the Proposed Sensor

The sensor proposed is shown in Figure 1, which is designed to obtain the frequency difference between waveform under test and reference clock by measuring the time it takes the oscillator to be certain number of clock cycles faster or slower than the reference clock. As shown in Figure 1, this architecture is composed of frequently used standard cells, including a 4-gate $2n\pi$ phase detector, a counter, a timer, and a control logic. The reference clock is used to capture the waveform under test at FF1. The last two capture results are held by the two serially connected flip-flops (FF1 and FF2). A pulse occurs at the output of the AND-gate A1 when the value held by FF1 is 1 and the value held by FF2 is 0. This pulse marks the time point when the two waveforms at D and CK of FF1 align with each other again. In phase domain, there is another 2π phase difference occurring between the waveform under test and reference clock, and we call this event "a hit". Therefore, the time it takes the faster waveform to be 2π phase ahead of the slower waveform is given by the interval between two neighboring pulses at the output of gate A1.

The $n-bit$ counter is driven by the pulses at the output of gate A1. Before measurement, a $StartingValue$ is

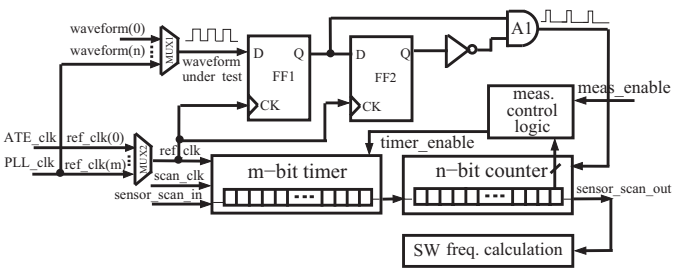


Figure 1: The architecture of Radic sensor.

shifted into the counter. The counter enables the timer when the $(StartingValue+1)th$ hit comes, and stops the timer when its most significant bit is 1 and all other bits are zero. By configuring the $n-bit$ counter with different $StartingValue$s, the sensor can measure the time it takes the two waveforms to have a $2\pi \times (Q-1)$ (Q is the overall hit count during measurement, and $Q = 2^{(n-1)} - StartingValue$) phase difference. According to the analysis in Section III, Radic's resolution can be controlled by changing the $StartingValue$ shifted into the counter.

The measurement window's length is recorded by the $m-bit$ timer by counting reference clock cycle number P. Before measurement, the timer will be reset to 0. Then, as mentioned above, it is enabled when the counter counts the $(StartingValue+1)th$ hit pulse and disabled when the counter's most significant bit is 1. After the measurement, the timer value will be scanned out to an off-chip memory or read to an on-chip memory.

Therefore at the end of measurement, there is $2\pi(Q-1)$ phase difference between the two waveforms. Radic allows the oscillator speed to be either slower or faster than reference clock. To simplify analysis, in this section, we only consider the slower case. Then the period of waveform under test (T_{os}) and reference clock (T_{refclk}) have the following relation:

$$T_{os} \times [P-(Q-1)] = T_{refclk} \times P \tag{1}$$

Therefore, the T_{os} can be calculated as:

$$T_{os} = \frac{T_{refclk} P}{P-(Q-1)} \tag{2}$$

The reference clock can either come from a stable external source (such as an ATE or a waveform generator) or an internal source such as a phase locked loop (PLL). If an internal clock source (such as PLL) is used as the reference clock, due to the aging of transistors, there is a chance its frequency can be degraded. To deal with reference clock frequency shifting, the proposed sensor performs the reference clock frequency measurement before any other measurement. As shown in Figure 1, during reference clock measurement mode, the PLL_clk will be chosen as waveform under test by $MUX1$, and an off-chip ATE clock (ATE_clk), or any other clock generated by signal generator, will be used as the reference clock (ref_clk) of the sensor. After the frequency measurement,

978-1-4673-1595-1/12/$31.00 ©2012 IEEE

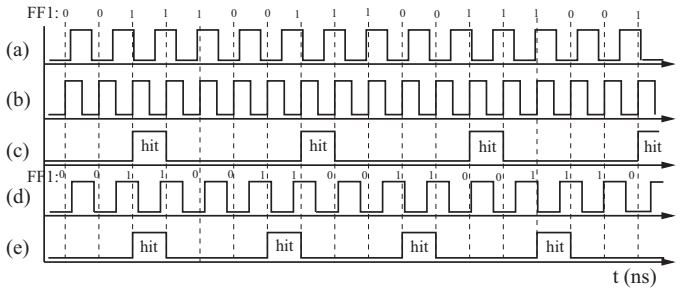


Figure 2: The waveform of 4-gate 2π phase detector (a) Waveform under test at time 0; (b) Reference clock waveform; (c) Output of gate A1 for fresh devices; (d) Waveform under test after stress time t_x; (e) Output of gate A1 at time t_x.

the PLL_clk can be used as a known frequency reference clock for other measurements. The waveforms under test can be any clock-like waveform on a chip. The usage of the sensor for aging and FF metastability measurements will be discussed in Subsections 2.1 and 2.2.

2.1 Using Radic for Aging Measurement

The sensor can be used for accurate aging measurement. $N_{2\pi}$ is defined as the number of reference clock cycles it takes the waveform under test and reference clock to have a 2π phase difference, and can be calculated by,

$$N_{2\pi} = \frac{1}{|1 - \frac{T_{refclk}}{T_{os}}|} \tag{3}$$

Assume initially $T_{os} > T_{refclk}$, and T_{os} will be increased further by aging. According to Equation 3, when the difference between T_{os} and T_{refclk} grows larger, it takes the two waveforms fewer cycles to have a 2π phase difference. Hence $N_{2\pi}$ will be changed due to aging. An illustrating example is shown in Figure 2. For fresh device (at time 0), as shown in Figures 2(a) and (c), it takes the reference clock (Figures 2(b)) 5 cycles to be another cycle faster than waveform under test. However, when aged for time t_x, as shown in Figures 2(d) and (e), it takes 4 reference clock cycles.

The sensitivity of $N_{2\pi}$ to T_{os} change can be calculated by,

$$|\ \frac{\partial N_{2\pi}}{\partial T_{os}}\ | = |\ \frac{T_{refclk}}{(T_{os} - T_{refclk})^2}\ | \tag{4}$$

with,

$$|\ \frac{\partial N_{2\pi(Q-1)}}{\partial T_{os}}\ | = |\ \frac{T_{refclk}(Q-1)}{(T_{os} - T_{refclk})^2}\ | \tag{5}$$

where $N_{2\pi(Q-1)}$ is defined as the number of reference clock cycles it takes the waveform under test and reference clock to have a $2\pi(Q-1)$ phase difference. It is obvious that, with the difference, which equals to $T_{os} - T_{refclk}$, not comparable to T_{refclk}, and a large enough hit number Q, the sensitivity of $N_{2\pi(Q-1)}$ (counted by the timer) to path under test (PUT) aging can be extremely high. In our implementation, to achieve highest sensitivity, T_{refclk} is chosen to have less than 10% difference from T_{os} by setting an off-chip signal source, or configuring our on-chip PLL.

When the sensor is used for aging measurement, the waveforms under test can be generated by PUTs of either buffer/inverter/gate chains or replicas of critical paths. To form an oscillation loop, the start- and end-point of a path must be connected by a loop-back wire with an odd number of inverting stages in the loop. For a critical-path-replica based loop, the off-path inputs needed to be set as non-controlling values by connecting the input to either VDD or VSS. And the oscillation period degradation is twice that of the PUT delay degradation, since loop-back wire will not be affected by NBTI or HCI. During stress, this loop can either be kept oscillating or broken. The PUT can be stressed under many conditions, four of them are shown in Figure 3. In Figure 3(a), the loop is broken, and the path is statically stressed. When the loop is kept during stress, the PUT will keep oscillating and is dynamic stressed, which is shown in Figure 3(b). Figure 3(c) shows a case when random values mimicking a real SOC signal are fed through the PUT with loop being broken, and the PUT can be randomly dynamically stressed. Finally in Figure 3(d), the power supply of the PUT can be toggled on and off by ATE or circuitry on the chip.

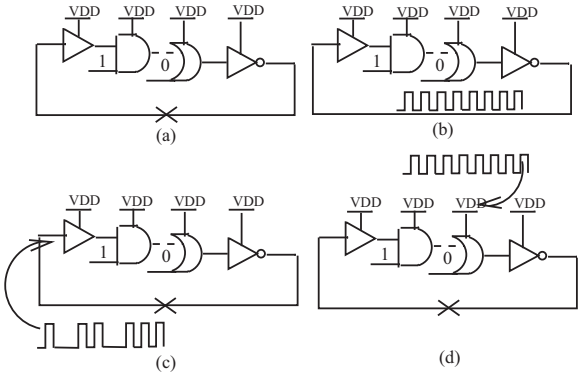


Figure 3: Four stress modes can be applied to a PUT. (a) Static stress with input stuck-at 0, (b) Dynamic stress with PUT oscillating, (c) Dynamic stress with random values mimicking a SOC signal fed to PUT input by FF4, and (d) Dynamic stress with power toggling.

2.2 Using Radic for Flip-flop Metastability Window Measurement

The experimental setting for FF metastability window measurement is shown in Figure 4. Flip-flop under test replaces FF1 in Figure 1, and $MUX3$ selects the FF under test. A free-running frequency controllable waveform and a reference clock waveform are fed to the data and clock pin of FF under test respectively. An extra $p - bit$ NBTI counter is assigned to count the free-running frequency controllable waveform.

978-1-4673-1595-1/12/$31.00

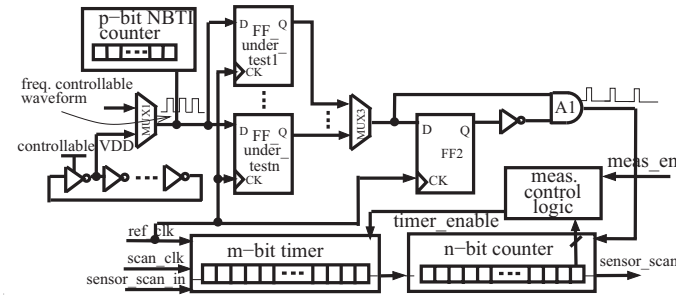


Figure 4: The use of Radic for FF metastability window measurement.

To trigger the metastability of a FF, the arrival time between data and clock edges should be smaller than the metastability window. For Radic, when the period difference (ΔT) of free-running frequency controllable waveform period T_{os} (supplied to the data pin of FF under test) and reference clock period T_{refclk} (supplied to the clock pin of the FF under test) is smaller than the metastability window T_w, the flip-flop metastability will be triggered. Figure 5 shows the relative rising edge locations of the free-running frequency controllable waveform and the waveform of clock when they are hitting each other. It is assumed that at $cycle_n$, the two waveforms are about to trigger the FF under test's metastability. Figure 5(a) shows the $\Delta T > T_w$ case. In this case, a fake 0-to-1 transition may or may not occur at $cycle_{n+1}$ due to FF under test's abnormal behavior inside metastability window. If the fake transition occurs in $cycle_{n+1}$, there will be no 0-to-1 transition in $cycle_{n+2}$, since the clock has moved outside the window in only one cycle, with $\Delta T > T_w$, and the captured value is 1 for sure. If there is no fake transition in $cycle_{n+1}$, a 0-to-1 transition will definitely occur in $cycle_{n+2}$. Therefore, in this case, whether the fake transition happens at $cycle_{n+1}$ or not, there will be overall one 0-to-1 transition when the two waveforms are hitting each other.

By continuously shrinking the frequency difference of the waveforms, Figure 5(b) shows the $\Delta T \leq T_w$ case. In this case, at $cycle_n$ and $cycle_{n+3}$, the relative phase difference between data and clock waveforms is larger than the metastability window, therefore the FF under test captured values are fixed 0 for $cycle_n$ and 1 for $cycle_{n+3}$. However, $cycle_{n+1}$ and $cycle_{n+2}$ both fall into the metastability window. According to the transition chart in Figure 5(b), it is possible that 2 0-to-1 transitions are generated before $cycle_{n+3}$. It is obvious that the smaller the frequency difference between FF's data and clock waveforms is, the more cycles will fall into the metastability window, and the high probability of multiple 0-to-1 transitions are generated when the two waveforms are hitting each other.

The multiple 0-to-1 transitions during the two waveforms are hitting each other is the "mark" for metastability window triggering, and will be found by comparing the sensor's counter, timer and NBTI counter values. When there is a hit, the two waveforms are having another 2π phase difference. It also means the difference between the value

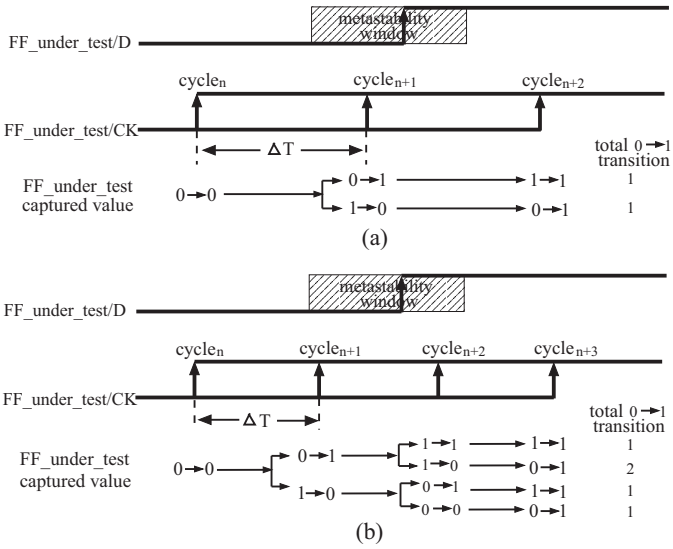


Figure 5: The relative phase difference between frequency controllable and the reference clock waveform when they are hitting each other, and the total 0-to-1 transition count for each possible case due to FF under test's metastability. (a) The $\Delta T > T_w$ case; (b) The $\Delta T \leq T_w$ case.

R of $p-bit$ NBTI counter, which counts the frequency controllable free-running waveform, and P of the $m-bit$ timer, which counts the reference clock waveform, becomes larger by 1, For the $\Delta T > T_w$ case, their relationship is always,

$$\mid R - P \mid = Q \tag{6}$$

where Q is the total number of 0-to-1 transitions counted by the $n-bit$ counter. As gate A1 always generate a pulse for each 0-to-1 transition, and the pulse is counted by the $n-bit$ counter. However, for the $\Delta T < T_w$ case, 1, 2 or even more 0-to-1 transitions might be generated in one hit, depending on how close the frequencies are. Therefore,

$$\mid R - P \mid \leq Q \tag{7}$$

By tweaking frequency controllable waveform's frequency towards the reference clock frequency and running the test, the metastability window's length will be found when Equation 7 is satisfied for the first time. The measured metastability window length T_{w_meas} is the period difference of the two waveforms, and can be calculated by,

$$T_{w\_meas} = \mid \frac{P \cdot T_{refclk}}{R} - T_{refclk} \mid \tag{8}$$

According to [7], when frequency tweaking step $\rightarrow 0$, and metastability repetition time (measurement time) $\rightarrow \infty$, the T_{w_meas} is approaching the real T_w by,

$$\lim_{T \rightarrow 0, P \rightarrow \infty} T_{w\_meas} \rightarrow T_w \tag{9}$$

As shown in Figure 4, there are multiple ways to obtain the frequency controllable waveform to run the test,

978-1-4673-1595-1/12/$31.00 ©2012 IEEE

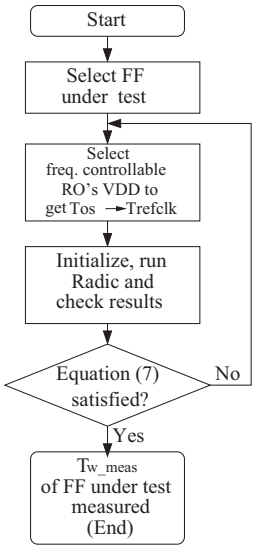


Figure 6: FF metastability window measurement flow.

which can either come from an on-chip oscillator with adjustable power supply, or from an off-chip waveform generator. In our experiment, an on-chip oscillator with adjustable power supply is used as the frequency controllable waveform source, which eliminates the cost of off-chip waveform generator. As expected, the frequency of an oscillator increases with decrease in power supply. According to the measurement of our implemented ring oscillators, their period can be changed in less than 1 pico second step, by connecting and tweaking a power supply with 0.001V accuracy.

The whole FF metastability window measurement flow is shown in Figure 6.

3 Analyzing Radic's Sensitivity

3.1 The Accuracy of Frequency Measurement

By comparing with the traditional counter-timer frequency measurement architectures [22] [23], where counter counts waveform under test and timer counts clock waveform, Radic provides much higher accuracy in the same measurement time, or achieves similar accuracy in a much shorter measurement time. The waveform under test's period measured by a traditional counter-timer can be calculated as:

$$T_{os} = \frac{M \cdot T_{refclk}}{N} \tag{10}$$

where N is the waveform under test cycles counted in M reference clock cycles, and its accuracy can be obtained by Equation 11:

$$Error_{trad} \leq \frac{M \cdot T_{refclk}}{N-1} - \frac{M \cdot T_{refclk}}{N} = \frac{M \cdot T_{refclk}}{N(N-1)} \tag{11}$$

However, Radic runs for Q_{th} hits (counted by the counter) during each measurement. And P (counted by the timer) is the number of reference clock cycles the measurement lasts. The waveform under test's period can be calculated by Equation 2. Due to the arrival time of the measurement end signal, the P value can be over or under counted by 1. Therefore, the error of Radic $Error_{RM}$ can be bounded by:

$$\begin{aligned} Error_{RM} &\leq \frac{T_{refclk}(P-1)}{(P-1)-(Q-1)} - \frac{T_{refclk}P}{P-(Q-1)} \\ &= \frac{T_{refclk}(Q-1)}{(P-Q)(P-Q+1)} \end{aligned} \tag{12}$$

If Q =2, which means the measurement lasts for 2 hits, the error of Radic can be expressed as:

$$Error_{RM}|_{Q=2} \leq \frac{T_{refclk}}{(P|_{Q=2}-2)(P|_{Q=2}-1)} \tag{13}$$

and if $Q = q$ $(q > 2)$,

$$Error_{RM}|_{Q=q} \leq \frac{T_{refclk}(q-1)}{(P|_{Q=q}-q)(P|_{Q=q}-q+1)} \tag{14}$$

It is obvious that the time interval between two hits is almost the same. Therefore, $P|_{Q=q}/P|_{Q=2} \approx (q-1)/(2-1) = q-1$. Substitute it into Equation 15, and consider $Q \ll P$. Hence,

$$\begin{aligned} \frac{Error_{RM}|_{Q=q}}{Error_{RM}|_{Q=2}} &= \frac{(q-1)(P|_{Q=2}-2)(P|_{Q=2}-1)}{(P|_{Q=q}-q)(P|_{Q=q}-q+1)} \\ &\approx 1/(q-1) \end{aligned} \tag{15}$$

This means that by increasing Q, which is determined by the value pre-scanned into the counter, the accuracy increases significantly.

Even with $Q = 2$, given same measurement time window (let $P = M$), and substitute N by Equation 10, by comparing Equation 13 and 11, we can get

$$\frac{Error_{RM}|_{Q=2}}{Error_{trad}} = \frac{\frac{T_{refclk}}{(P-2)(P-1)}}{\frac{MT_{refclk}}{N(N-1)}} \approx \frac{1}{P}(\frac{T_{ref}}{T_{os}})^2 \tag{16}$$

When T_{os} and T_{refclk} are comparable, according to 16, the accuracy is improved by almost P times. And the accuracy can be further improved by increasing Q according to Equation 15.

As the counter in Radic counts the hit, the switching activity of the counter is $1/P|_{Q=2}$ of the traditional counter-timer frequency sensors. Therefore, Radic's power consumption is much smaller. In summary, Radic can obtain much better accuracy and consume less power in the same measurement time.

Figure 7 shows the accuracy of traditional counter-timer architecture and that of Radic both on our chip. It can

978-1-4673-1595-1/12/$31.00

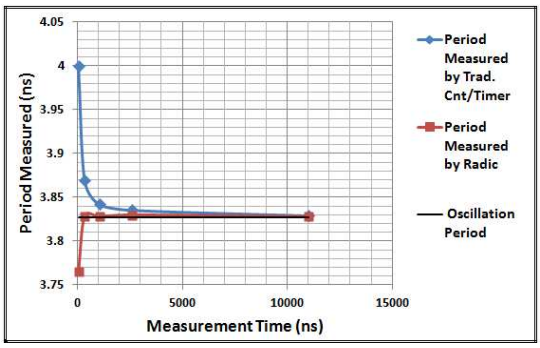


Figure 7: Accuracy comparison between the fabricated traditional counter-timer and Radic measurement results.

be seen that Radic reaches a high resolution within 500ns, while it takes the traditional counter-timer architecture more than 3000ns to reach the same resolution. By using Radic, the recovery of DC-NBTI aging can be minimized by performing measurement in a much shorter time.

3.2 The Accuracy of Setup Time Measurement

In frequency measurement mode, the reference clock frequency is not allowed to be too close to the waveform under test's to avoid FF1's metastability window. However, in metastability measurement mode, the controllable waveform source's frequency is approaching the reference clock's to trigger the metastability behavior of the FF under test. According to Equation 8, the accuracy of the sensor is,

$$Error_{T_{w\_meas}} \leq \frac{P \cdot T_{refclk}}{R(R-1)} \tag{17}$$

and this error can be reduced by increasing measurement time.

3.3 The Aging/Process Robustness

The aging and process variations of the sensor itself do not affect the frequency measurement accuracy. This can be verified by checking aging/process's effects on every parameter in Equation 2. To guarantee the known reference clock (T_{refclk}) is the same as what is on silicon, it can either be measured by the proposed sensor itself in clock measurement mode, or provided by an off-chip clock source. Then the timer will be started at the first hit, and be stopped after certain number of hits. If the aging and process variation are not large enough to generate defects, the timer and counter counting process are all aging/process robust. Hence, all values in frequency-calculation Equation 2 measured by the Radic sensor are robust in presence of aging and process variation. Similarly, in Equation 8, all parameter on the right side of the metastability-calculation equation are aging/process robust.

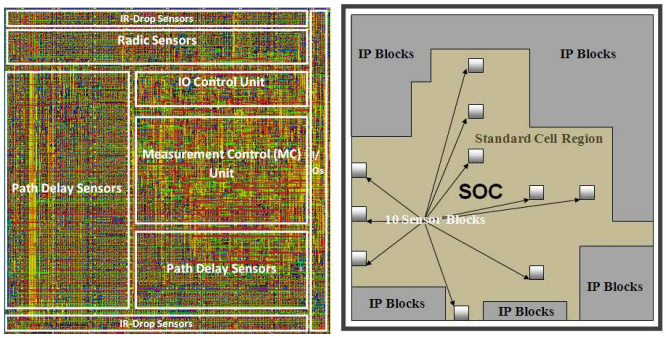
Table 1: PUT Assignments

PUT	Individual Cell Threshold Voltage	Individual Cell Gate Size	PUT Stage Count	Stress Type
OS0	High	Large	81	DC/AC
OS1	Low	Large	121	DC/AC
OS2	High	Small	45	DC/AC
OS3	Low	Small	75	DC/AC

4 Silicon implementation and Results

A sensor block containing Radic has been designed and fabricated in a very advanced technology Freescale SOC as shown in Figure 8(a). 10 identical sensor blocks are placed at different locations within the SOC chip as shown in Figure 8(b). Four different ring oscillators are hooked to Radic as PUTs for aging degradation measurement. The detail of the four ring oscillator PUTs are shown in Table I. 80 FFs spread all over the die are connected to Radic for metastability window measurement.

The target period measurement accuracy is 0.1ps. After several trial runs with different counter value Qs chosen before, and timer value Ps obtained after the trial runs, the minimum Q which satisfies the targeted accuracy can be found according to Equation 12.



(a) The sensor block containing Radic.

(b) Locations of the 10 sensor blocks on SOC.

Figure 8: Implemented sensor block and SOC overview. Note that, the sensor block contains many other sensors that are outside the scope of this paper.

The control signals of the SOC under test comes from another Freescale 32-bit micro-controller chip. The test and measurement infrastructure is shown in Figure 9. Temperature control equipment is used to accelerate the aging process.

4.1 Design, Test Cost, and Area Overhead

Radic contains a 4-gate 2π phase detector, a 12-bit counter, a 13-bit timer, a 12-bit NBTI counter, and a small measurement control logic. As the sensor is composed by the most ordinary standard cells, driven by the SOC system clock, and there is no distance requirement between PUT and Radic, Radic can be automatically synthesized, placed, and scan inserted by any commercial EDA

978-1-4673-1595-1/12/$31.00 ©2012 IEEE

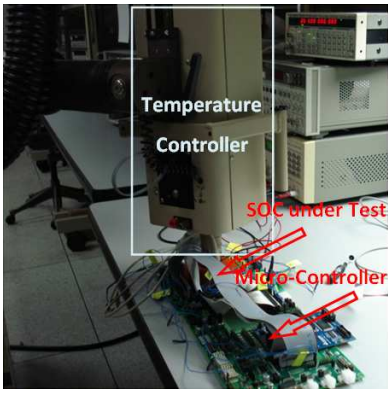


Figure 9: Test and measurement setup.

Table 2: Comparison of Sensor and Oscilloscope Results (ns)

PUT	Fresh IC			Stressed IC		
	Radic	Osci.	Error%	Radic	Osci.	Error%
OS0	2.6115	2.6116	0.002%	2.6369	2.6368	0.003%
OS1	2.2161	2.2163	0.007%	2.2398	2.2397	0.004%
OS2	2.4886	2.4888	0.004%	2.5063	2.5062	0.004%
OS3	2.2611	2.2609	0.007%	2.2811	2.2813	0.007%

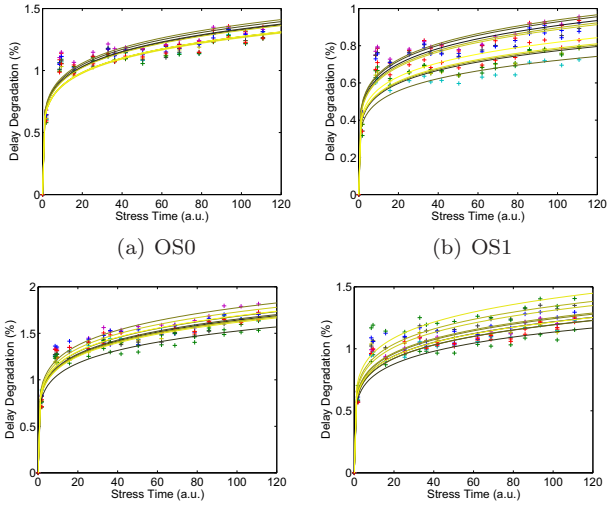
tools. The ATPG tools used during implementation generate stuck-at patterns with coverage higher than 97%. Including the 4 PUTs mentioned above, the overall layout gate count is less than 1.5k. As composed by only standard cells, and Radic has no requirements about gate size, the actual area overhead per sensor block is 0.004%. And the overall area overhead for 10 sensor blocks is 0.04%. Hence the sensor proposed has extremely low silicon cost.

4.2 Accuracy Verification by Comparing with Oscilloscope Results

The PUT delay (half of the oscillation period) measured internally by Radic and externally by oscilloscope are compared in Table II. To minimize the measurement noise from the oscilloscope, multiple measurements are done and average results are reported. The highest accuracy of the oscilloscope used is 0.01ns; to further improve the accuracy, the frequency of PUT is divided by 32 by an in-sensor frequency divider before measured by the oscilloscope. Hence the accuracy of the oscilloscope is improved to 0.3ps. Columns 2-4 in the table show the measurements when the device is fresh (time 0), while the last three columns show the results for the stressed device. When under stress, the whole SOC was stressed under 125^oC and elevated power supply of 1.8V for more than 1×10^4 seconds. The Error columns show the difference between Radic and oscilloscope results for fresh and stressed ICs. The extremely small error rates demonstrate the sensor's high accuracy and aging robustness.

4.3 Aging Measurement Results

After Radic's accuracy has been verified, the sensor is used to measure the aging degradation trend of cells with different driving abilities and threshold voltages as shown in Table I. Figure 10 shows the measured long-term delay



(a) OS0 (b) OS1

(c) OS2 (d) OS3

Figure 10: Aging measurement of four PUTs (OS0, OS1, OS2, and OS3) with 125^oC and 1.8V (DC Stress). Each subfigure shows the results of the 10 replicas of each PUT locating in 10 sensor blocks. Hence the difference of the 10 curves in each subfigure reflects the intra-die process variation for certain cell type.

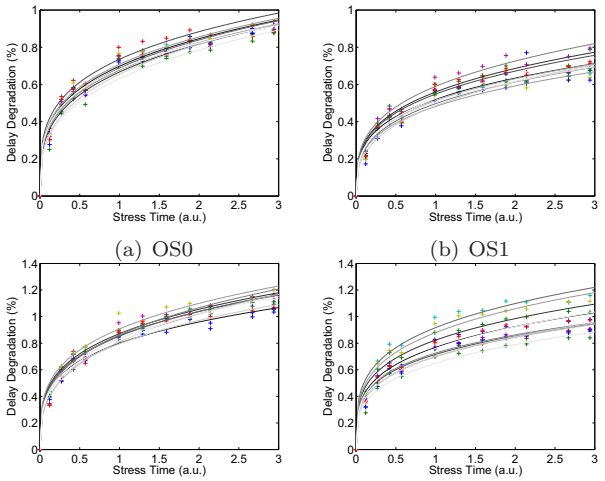
degradations of the PUTs under DC stress at 125^oC and 1.8V. Similar to threshold voltage, PUT's delay degradation also has a power-law dependence on stress time. In other words, the depencency can be descript as $\Delta d = At^n$, where A is a constant, and t is the stress time. The power-law equations obtained by curve fitting indicate time exponents of 0.14 to 0.16. According to our data, small standard cells in OS2 with high time-zero threshold voltages has larger average delay degradation percentage of 1.8%. On the other hand, large cells in OS1 with low threshold voltages has the lowest delay degradation percentage of 0.8%. The average delay degradation for OS0 and OS3 cells are both 1.2%.

Also notice from Figure 10 that the first measurement results all stay outside the fitting curve for all PUTs. The degradation characteristics at the early aging stage is then presented. Figure 11 shows the measured delay degradation for the same PUTs as in Figure 10 but for the first 1/40 length of long-term aging. The power laws measured for this short term aging are as high as 0.27 to 0.3.

Figure 10 and Figure 11 show two distinct slopes which indicate two different time-dependent mechanisms at different phases of NBTI aging. The early phase time-power law of 0.27-0.3 extracted from Figure 11 matched the hydrogen-oxygen interface bond breaking/trap theory [24]. While the long term time-power law of 0.14-0.16 extracted from Figure 10 matches hydrogen diffusion theory [25].

Real paths are seldom under continuous DC stress. A typical product undergoes both dynamic and static stresses. When keeping the PUT oscillating during the entire stress period, NBTI, NBTI recovery, and HCI degradations will all take place. The two fundamental degradation models for NBTI and HCI differ in many respects. However, both of them involve the break of Si-H bonds at

978-1-4673-1595-1/12/$31.00 ©2012 IEEE



(a) OS0 (b) OS1

(c) OS2 (d) OS3

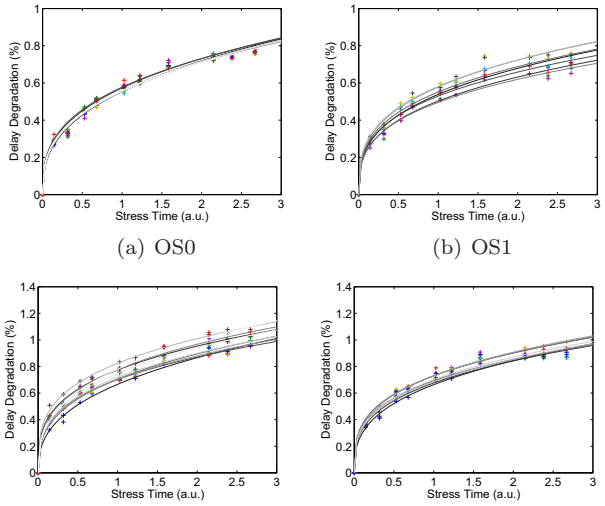
Figure 11: Early aging stage of aging measurement with 125^oC and 1.8V (DC Stress) taken from Figure 10.

the Si/Oxide interface followed by H diffusion in the oxide. Therefore, it is not surprising that the time-exponents of interface trap density of both NBTI and HCI can be bounded together.

Figure 12 shows the delay degradation of the PUTs with AC stress. Comparing with Figure 11 which has DC NBTI effect only, Figure 12 has a higher power law of 0.31 to 0.37. The power law increase is very likely due to the HCI effect when the PUT is AC stressed. In Figure 13, the delay degradation percentages are analyzed by comparing the same PUT under DC and AC stress. It can be seen that at first, due to the recoverable NBTI component, the degradation of the AC stressed PUT is smaller than DC-stressed one. However, as the time increases, the NBTI recovery weakens plus there is a measurable contribution from HCI, cause the delay degradation of the AC-stressed PUT to become larger than that of the DC-stressed PUT. This measurement shows that, in our technology, a path that frequently switches has a higher chance of failing due to the combined aging effects.

4.4 Flip-Flop Metastability Window Measurement Results

The frequency controllable oscillator used in this implementation has around 1ps period sweeping step, which can be obtained by tweaking a power supply with 0.001V step. The measurement is conducted according to the flow shown in Figure 6. The distribution of measured metastability window T_{w_meas} of the 80 FFs under test are shown in Figure 14. The measured metastability window varies from 46ps to 75ps across the die with an average of 61.5ps under 25^oC and 1.2V normal power supply. This result is used for reducing excessive setup/hold timing margin. To show process variation's significant impact on FF metastability window, Figure 15 compares the normalized FF metastability window and small high-threshold voltage inverter delay distribution of the same die. It can be seen that both distributions can be fitted by Gaussian curve. The FF metastability window distribution has a standard deviation of $\sigma = 0.1064$, however, the inverter delay distribution only has a σ of 0.0159. Hence FF's metastability window has a much higher variation percentage comparing with combinational-instance delay on the same SOC.



(a) OS0 (b) OS1

(c) OS2 (d) OS3

Figure 12: Delay degradation of OS0, OS1, OS2, and OS3 when they keep oscillating during stress of 125^oC and 1.8V (AC Stress).

5 Conclusion

In this paper, a new low-cost and accurate sensor called Radic is presented. By employing this sensor, we can perform purely on-chip frequency, aging, and metastability window measurements. The sensor is composed of a small number of standard cells, requires no modification to the design, DFT, and ATE test flows, and is able to achieve high accuracy within a short measurement time. The sensor has been fabricated on a Freescale design. The aging/process robustness of the sensor has been verified on silicon by comparing with oscilloscope results. The silicon aging measurement results accurately agree upon aging models, which also demonstrate its accuracy. The FF metastability windows widths across the die are measured, which are found to be very sensitive to process variations. The results obtained can greatly help design and test engineers to deal with timing margin more efficiently. As part of our future work, we plan on using this sensor on critical-path replicas which are stressed by power supplies

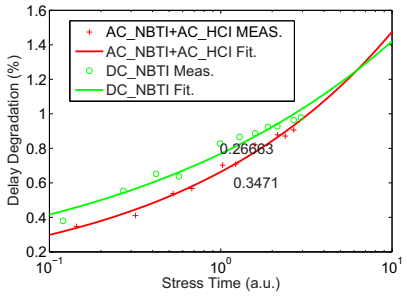


Figure 13: Delay degradation of DC and AC stressed OS0.

978-1-4673-1595-1/12/$31.00 ©2012 IEEE

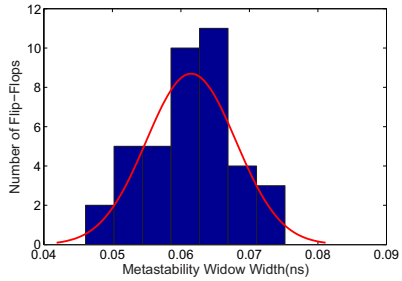


Figure 14: The distribution of metastability window widths for the 80 FFs under test.

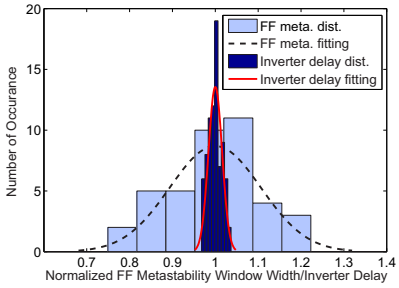


Figure 15: The comparison between normalized FF metastability window width and inverter delay distributions.

and inputs mimicking the real critical paths' to perform in-field SOC self aging adaptation.

References

[1] W. Abadeer and W. Tonti, "Bias temperature reliability of N^+ and P^+ polysilicon gated NMOSFETs and PMOSFETs," in Proc. *IEEE Int. Reliability Physics Symp.'93*, pp. 147-149, 1993.

[2] M.A. Alama, H. Kufluoglua, D. Varghesea, b and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation: Recent progress," *Microelectronics Reliability*, Vol. 47, pp. 853-862, 2007.

[3] E. Takeda, Y. Nakagome, H. Kume, S. Asai, "New hot-carrier injection and device degradation in submicron MOSFETs," *IEE Solid-State and Electron Devices*, volume 130, pp. 144-150, 1983.

[4] T. Ohnakado, K. Mitsunaga, M. Nunoshita et al., "Novel electron injection method using band-to-band tunneling induced hot electrons (BBHE) for flash memory with a P-channel cell," in Proc. *International Electron Devices Meeting*, pp. 279-282, 1995.

[5] P. Heremans, R. Bellens, G. Groeseneken and H. Meas, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs" *IEEE Trans. Electron Devices*, volume 35, no. 12, pp. 2194-2209, 1988.

[6] "http://www.itrs.net/Links/2011ITRS/Home2011.htm"

[7] C. Dike and E. Burton, " Miller and Noise Effects in a Synchronizing Flip-Flop," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 6, pp. 146-157, 1989.

[8] K. Kang, K. Kim, A. Islam, M. Alam, and K. Roy "Characterization and Estimation of Circuit Reliability Degradation under NBTI using On-Line I_{DDQ} Measurement," in Proc. *DAC'07*, 2007.

[9] M. Li, D. Huang, C. Shen, T. Yang, W. Liu, and Z. Liu, " Understand NBTI Mechanism by Developing Novel Measurement Techniques," *IEEE Transactions on Device and Materials Reliability*, 2008.

[10] J. Keane, T. Kim and C. Kim, "An On-Chip NBTI Sensor for Measuring pMOS Threshold Voltage Degradation," *IEEE VLSI Systems*, pp. 947-956, 2007.

[11] M. Agarwal, B. Paul, M. Zhang, S. Mitra "Circuit Failure Prediction and Its Application to Transistor Aging," *IEEE VTS'07*, pp. 1-8, 2007.

[12] A. Cabe, Z. Qi et al, "Small Embeddable NBTI Sensors (SENS) for Tracking On-Chip Performance Decay," in Proc. *ISQED'09*, pp. 1-6, 2009.

[13] K. K. Kim, W. Wang, K. Choi, et al., " On-Chip Aging Sensor Circuits for Reliable Nanometer MOSFET Digital Circuits," *IEEE Trans. on Circuits and Systems*, pp. 798-802, 2010.

[14] P. Singh, E. Karl, D. Sylvester, and D. Blaauw, et al., "Dynamic NBTI management using a 45nm multi-degradation sensor ," in Proc. *CICC'10*, 2010.

[15] J. Vaquez, V. Champac, et al., "Predictive Error Detection by On-Line Aging Monitoring," in Proc. *IEEE Int. On-Line Testing Symp.*, pp. 9-14, 2010.

[16] M. Omana, D. Rossi, N. Bosio, C. Metra, et al., "Self-Checking Monitor for NBTI Due Degradation," in Proc. *IEEE 16th International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW)*, 2010.

[17] M. Agarwal, V. Balakrishnan, A. Bhuyan, et al., "Optimized Circuit Failure Prediction for Aging: Practicality and Promise," in Proc. *ITC'10*, 2010.

[18] E. Karl, P. Singh et al, "Compact In-Situ Sensors for Monitoring Negative-Bias-Temperature-Instability Effect and Oxide Degradation," in Proc. *ISSCC'08*, pp. 410-412, 2008.

[19] J. Horstmann, H. EICHEL, and R. COATES, " Metastability Behavior of CMOS ASIC Flip-Flops in Theory and Test," *IEEE Journal of Solid-State Circuits*, Vol. 24, pp. 146-157, 1989.

[20] D. Kinniment, K. Heron, and G. Russell, "Measuring Deep Metastability," in Proc. *ASYNC06*, pp1-10, 2006.

[21] A. Cantoni, J. Walker, and T. Tomlin " Characterization of a Flip-Flop Metastability Measurement Method," *IEEE Journal of Solid-State Circuits*, Vol. 24, pp. 146-157, 1989.

[22] K. Arabi, H. Ihs, C. Dufaza and B. Kaminska, "Dynamic digital integrated circuit testing using oscillation-test method," *Electronics Letters*, pp. 762-764, April 1998.

[23] W. Wu, C. Lee, M. Wu, J. Chen and M. Abadir, "Oscillation ring delay test for high performance microprocessors" *Journal of Electronic Testing*, vol 16, no. 1-2, pp. 147-155, Feb. 2000.

[24] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, "A comprehensive framework for predictive modeling of negative bias temperature instability," in Proc. *IRPS'04*, pp. 273-283, 2004.

[25] H. Reisinger et al., " Comparison of Very Fast to Very Slow Components in Degradation and Recovery Due to NBTI and Bulk Hole Trapping to Existing Physical Models," *IEEE Trans. on Device and Materials Rel.*, pp. 119-129, 2007.

978-1-4673-1595-1/12/$31.00