A Novel Flow for Reducing Clock Skew Considering NBTI Effect and Process Variations

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Abstract

Negative bias temperature instability (NBTI) has emerged as a major concern not only to the functional circuits, but also to the clock tree. Further aggravated by process variations, aging-induced reliability issue becomes more challenging when technology further scales. Development of effective solutions for reducing clock skew and compensating aging effect under process variations remains as a challenge. Taking the impact from NBTI and process variations into account, we propose a novel flow for reducing clock skew by selectively replacing standard-V_{th} clock buffers with their high-V_{th} counterparts. An extended "divide and conquer" algorithm is developed to identify the critical clock buffers for replacement. The area overhead of our proposed flow is negligible, and the power consumption is reduced as well. Simulation results show that the proposed flow can effectively reduce the clock skew by at least 20% by replacing only 1.08% clock buffers on average for 10 years of degradation, even under an extremely constrained condition. The efficiency of our flow will be higher when the clock tree structure has a higher depth, rendering it more favorable for large-scale industry designs.

Keywords:

Aging, Process Variations, Clock Tree, Clock Skew

1. Introduction

The rapid scaling of CMOS technology has inevitably exacerbated the reliability issues, e.g. aging effects. Negative bias temperature instability (NBTI) is one of the most notable aging effects impacting circuit performance and reliability. NBTI is prominent in PMOS transistors, shifting the threshold voltage, reducing the drive current, and eventually failing the circuit. Circuit level simulations have demonstrated that NBTI can result in a 10% circuit delay degradation over 10 years of operation [1] [2]. Although NBTI impact on functional circuits has been extensively studied and various solutions were proposed, its impact on the clock tree has not been sufficiently examined yet. Process variation is another major concern in circuit design, as it deviates the performance of ICs from the design specification. Without carefully tackling these issues, yield can be negatively impacted. International technology roadmap for semiconductors (ITRS) estimated that the delay variability due to process variations would reach 49% in 2010, 63% in 2015, and continues to increase in future technology nodes [3].

Prior research focuses on the impact of capacitive loads, aging or process variations separately on clock skew. Some earlier research focused on zero-skew routing techniques. These techniques manipulate the clock skew, induced by capacitive load mismatch, using load-matching approaches [4] [5] [6]. Such techniques insert multiple types of control gates into the clock tree to gate the clock paths, which is defined as clock signal path from the source clock to a sink D flip-flop. However, the clock skew remained difficult to control due to the different types of logic gates and buffers used, resulting in capacitive load mismatch. Similarly, process variations cannot be avoided. Although power consumption may be reduced as an optimization objective, these techniques fail to completely address the skew problem. For example, the authors in [7] added extra circuitry to simplify clock control logic in order to reduce the clock skew. However, their scheme was not applicable to all implementations, and the power consumption was not optimized without gating off the unnecessary clock switching [8]. More importantly, process variation was not taken into account in these approaches. The authors in [9] comprehensively analyzed the impact of process variations on the clock skew. Their results confirmed that process variation is a significant source of clock skew in deep sub-micron technology nodes. Clock tree routing algorithms have been proposed in literature to improve skew tolerance to process variations. The authors in [10] estimated the worst-case skew under process variations, and employed it to guide the decision-making during the routing procedure. Similar methodologies were proposed in [11] [12]; however few of them paid attention to aging effects, which is another dominant source for inducing clock skew, especially in smaller technology nodes.

The authors in [13] proposed a solution to reduce clock skew due to NBTI. By calculating the clock skew degradation induced by NBTI, the clock signal on the corresponding path was guardbanded with a safety margin. The safety margin is set as exactly half of the skew degradation, thus the skew was constrained for a lifetime operation. Although process variations were taken into account, this methodology was limited by its safety margin, which could not exceed half of the skew degradation. The authors in [14] tried to equalize the signal probability of all clock paths according to runtime operation, and could achieve a significant reduction of clock skew induced by NBTI. However, their scheme assumed a relatively ideal condition where the process variations were not considered. The authors in [15] proposed an optimization algorithm to select NAND or NOR gate as the output stage of the integrated clock gating (ICG) cells. This enabled the control of ICG output signal to remain at "0" or "1", thus balancing the degradation rate of clock paths and minimize NBTI induced clock skew. Similarly, the authors did not consider the impact of process variations. In addition, this method lacked a comprehensive analysis on the fanout condition of clock gating. As an example, the clock path with the worst degradation (we call it the fastest-degrading path or the worst

path) connected to an ICG cell may be slowed down by fixing the ICG cell output at "0" through the optimization procedure. However, this may expedite the degradation of another connected path, causing it to become the worst path. The method in [16] was essentially an inter-node-control (INC) scheme, which balanced the degradation rate of the clock paths by carefully manipulating the stress probabilities to the critical PMOS transistors. However, process variations were not considered, and that all control enable signals must be determined a priori.

In summary, there is little work to address the clock skew problem considering both the process variations and aging. Clock skew optimization considering aging is usually conducted separately on the assumption that the timing properties of the clock tree is already optimized considering the process variations. Consequently, margins based on process variations and aging are added up. This will over-pessimistically guardband the clock signal and lose performance excessively. Furthermore, most of the research attempt to optimize the clock skew through INC or similar methodologies by balancing the degradation rates of different clock paths. Therefore, the introduced area and power consumption of the control circuitry must be carefully considered to avoid large overhead. Meanwhile, it must be ensured that the INC schemes do not expedite the degradation of the slow-degrading paths to make a worst path.

In this paper, delay degradation of the clock buffers with different initial threshold voltages are accurately evaluated using the long-term NBTI predictive technology model (PTM), considering the impact of signal stress probabilities, and the stress and recovery mechanisms [1] [2]. A sub-library embracing the clock buffers in the standard cell library is characterized for multi-V_{th} consideration. We propose a novel clock skew reduction flow considering both NBTI and process variations. Our flow is a synthesis framework using the high-V_{th} buffers to replace the identified standard-V_{th} counterparts. Although the leakage power is not our optimization objective, our flow is effective in reducing the leakage power as well, since a high-V_{th} buffer has a smaller leakage current. We develop an extended "divided and conquer" algorithm to identify the clock buffers for replacement, using the static timing analysis information of the clock tree, and calculating the degradation information with the long-term NBTI model. To take process variations into account, we use the existing mathematical models to evaluate the mean and standard deviation of the delay of each high-V_{th} buffer. Differences from the mean delay and standard deviation of the original standard-V_{th} buffer will guide the decision-making to ensure that swapping buffers will effectively reduce the clock skew without violating the design specifications. Different from existing clock skew reduction methods, our flow does not change the clock tree connection and topology, inserting no extra control circuitry. More importantly, our flow does not aggravate the degradation rate of any clock path. In addition, our synthesis flow can work effectively without interrupting the current conventional design flow.

The rest of the paper is organized as follows. Section 2 presents the NBTI model, and the statistical prediction of NBTI under process variations will be derived from transistor-level to path-level. Section 3 describes the motivation behind our flow. Section 4 presents the details of our synthesis flow for clock skew reduction. Section 5 shows results on several benchmark circuits, and Section 6 concludes the paper.

2. NBTI Effect and Process Variations Characterization

This section presents NBTI model and its characterization under process variations. The models will be extensively studied to characterize the clock buffers considering different threshold voltages.

2.1. NBTI Effect Modeling

NBTI effect is commonly acknowledged as a result of the generation of interface charges at the Si–SiO_2 boundary, and is analytically interpreted using the reaction diffusion (R-D) model [17] [18]. Consequently, NBTI is highly dependent on the bias condition. A forward bias ($V_{gs} = -V_{dd}$, where V_{dd} is the supply voltage) accelerates the NBTI effect, which leads to an increase in the PMOS threshold voltage. However, a reverse bias ($V_{gs} = 0$) recovers NBTI effect partially, and decreases the absolute value of the threshold voltage. PTM model [2] captures the behavior of the alternate stress and recovery phases of the degradation of PMOS transistor. The corresponding long-term compact model is formulated as:

$$|\Delta V_{th}(t)| = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1-\beta_t^{1/2\phi}}\right)^{2\phi} \quad (1)$$

$$\beta_t = 1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(1-\alpha)T_{clk}}}{2t_{ox} + \sqrt{Ct}} \quad (2)$$

$$K_v = \left(\frac{q t_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}(V_{gs} - V_{th})\sqrt{C} exp\left(\frac{2E_{ox}}{E_o}\right) \quad (3)$$

where α is the duty ratio, and T_{clk} is the clock period. The other parameters are physical related constants. In the model, the random stress signal is converted into a rectangular waveform with duty ratio α, and $|\Delta V_{th}(t)|$ is a tight upper bound of the long-term degradation of the PMOS transistor [1] [2]. Thus, any long-term NBTI analysis can be successfully conducted using a deterministic duty ratio α obtained from the actual random stress signal. Additionally, Equation (1) demonstrates that $|\Delta V_{th}(t)|$ exponentially depends on initial threshold voltage V_{th}. It also manifests that a lower $|V_{th}|$ PMOS transistor has a faster degradation rate, and thus a larger $\Delta V_{th}(t)$ increase [2]. Alpha-power law [21] provides an analytical model between V_{th}, $\Delta V_{th}(t)$ and gate-level delay D_i as:

$$D_i = \frac{C_i V_{dd}}{\beta_i [V_{dd} - (V_{th} + \Delta V_{th}(t))]^\gamma} \quad (4)$$

where C_i is the effective capacitive load connected to the gate i, and β_i is a parameter depending on the gate size. We simulate clock buffers from the 45nm Nangate Cell Library using the PTM model and PTM transistor parameter values [20]. Our results on a minimum-sized buffer shown in Figure 1 illustrate that buffers with lower initial V_{th} tend to degrade faster, while those with a higher initial V_{th} have a slower degradation rate. Such an argument can be made for other gate types as well [19] [22].

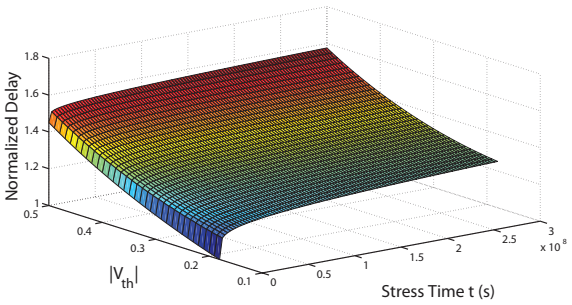


Fig. 1. Normalized delay of a minimum-sized clock buffer versus initial threshold voltage V_{th} and stress time t ($\alpha = 0.5$, and temperature $T = 125^oC$).

2.2. Statistical Prediction of NBTI Effect under Process Variations

In this section, we will propose the circuit-level model for path and clock-tree delay analysis. Delays and degradations of paths, when their cell components have different initial threshold voltages, will be compared and the difference will be modeled. Additionally, clock skew will finally be formulated.

Using the first-order Taylor Expansion of $1/(1-x)^{\alpha} \approx 1+\alpha x$ (when $|x| \ll 1$), Equation (4) can be reformulated as:

$$D_i = D_{i0} \times (1 + S_{ti} \times \Delta V_{th}(t)) \quad (5)$$
$$D_{i0} = C_i V_{dd}/[\beta_i \times (V_{dd} - V_{th})^{\gamma}] \quad (6)$$
$$S_{ti} = \frac{\gamma}{(V_{dd} - V_{th})} \quad (7)$$

where D_{i0} is the gate delay without process variations and NBTI degradation, with $\Delta V_{th}(0) = 0$. From Equation (5), we can see that $S_{ti} \times \Delta V_{th}(t)$ decreases with the increase in the initial threshold voltage V_{th}, demonstrating that gates with lower initial V_{th} tend to degrade faster, while those with higher initial V_{th} have slower degradation rate.

To take process variations into account, the mean value $\mu_{D_i}(t)$ and standard deviation $\sigma_{D_i}(t)$ of the gate delay at time t can be formulated as [22]:

$$\mu_{D_i}(t) = \mu_{D_i}(0) \times (1 + AS_{ti}t^{\gamma}) \quad (8)$$
$$\sigma_{D_i}(t) = \sigma_{D_i}(0) \times (1 - AS_v t^{\gamma}) \quad (9)$$
$$\mu_{D_i}(0) = D_{i0} \quad (10)$$
$$\sigma_{D_i}(0) = D_{i0} S_{ti} \sigma_{pvi} \quad (11)$$

where A and S_v are positive values, whose values are dependent on the technology features and remain as constants under the specific operating condition.

Since standard deviation of the delay is always a positive value, we can see that $0 \leq 1 - AS_v t^n \leq 1$. Comparing Equation (8) with Equation (5), it satisfies that AS_{ti} decreases when V_{th} increases. Equations (8) through (11) formulate the gate delay considering NBTI degradation under process variations. By treating a path as a concatenation of K gates on it, the mean value and standard deviation of the path delay can be formulated as:

$$\mu(0) = \tau_0 \quad (12)$$
$$\sigma(0) = \tau_0 S_{ti} \sigma_{pv} \quad (13)$$
$$\sigma_{pv} = \sqrt{\sum_{i=1}^{K} \sigma_{pvi} + \sum_{\substack{1 \leq i \leq K \\ 1 \leq j \leq K \\ i \neq j}} \sum 2\rho_{pvij}\sigma_{pvi}\sigma_{pvj}} \quad (14)$$
$$\mu(t) = \mu(0)(1 + AS_{ti}t^{\gamma}) \quad (15)$$
$$\sigma(t) = \sigma(0)(1 - AS_v t^{\gamma}) \quad (16)$$

where $\mu(0)$ $(= \tau_0)$ is mean value of the path delay at time 0 without NBTI degradation; $\sigma(0)$ is the corresponding standard deviation; $\mu(t)$ and $\sigma(t)$ are the mean delay and standard deviation at time t; σ_{pvi} is the standard deviation of the delay of gate i; ρ_{pvij} is the correlation between ΔV_{th_pvi} and ΔV_{th_pvj}.

Equations (12) through (16) formulate the mean value and standard deviation of the path delay considering NBTI degradation under process variations. Let us assume that, at time t, the mean value and standard deviation of the delay of paths m and n are $(\mu_m(t), \sigma_m(t))$ and $(\mu_n(t), \sigma_n(t))$ respectively. If they have the correlation ρ_{mn}, the delay difference between them will satisfy a distribution having the mean value $\Delta\mu(t)$ and standard deviation $\Delta\sigma(t)$, which can be formulated as:

$$|\Delta\mu(t)| = |\mu_m(t) - \mu_n(t)| \quad (17)$$
$$\Delta\sigma(t) = \sqrt{\sigma_m^2(t) + \sigma_n^2(t) - 2\rho_{mn}\sigma_m(t)\sigma_n(t)} \quad (18)$$

From Equations (17) and (18), the delay difference $\Delta\tau$ between paths m and n (at time t) is upper-bounded as:

$$\begin{aligned}
\Delta\tau &\leq |\Delta\mu(t)| + |\Delta\sigma(t)| \\
&= |\mu_m(t) - \mu_n(t)| \\
&\quad + |\sqrt{\sigma_m^2(t) + \sigma_n^2(t) - 2\rho_{mn}\sigma_m(t)\sigma_n(t)}| \\
&= |\mu_m(t) - \mu_n(t)| \\
&\quad + |\sqrt{\sigma_m^2(0) + \sigma_n^2(0) - 2\rho_{mn}\sigma_m(0)\sigma_n(0)} \\
&\quad \times (1 - AS_v t^{\gamma})| \\
&\leq |\mu_m(0) \times (1 + AS_{tim}t^{\gamma}) - \mu_n(0) \times (1 + AS_{tim}t^{\gamma})| \\
&\quad + |\sqrt{\sigma_m^2(0) + \sigma_n^2(0) - 2\rho_{mn}\sigma_m(0)\sigma_n(0)}| \\
&\leq |\mu_m(0) - \mu_n(0) \\
&\quad + t^{\gamma} \times [AS_{tim} \cdot \mu_m(0) - AS_{tin} \cdot \mu_n(0)]| \\
&\quad + |\sqrt{\sigma_m^2(0) + \sigma_n^2(0) - 2\rho_{mn}\sigma_m(0)\sigma_n(0)}| \quad (19)
\end{aligned}$$

Thus, we can conclude that the delay difference between two paths can be upper-bounded mathematically considering both NBTI degradation and process variations. For a clock tree consisting of a large number of paths, $Max(\Delta\tau_{i,j})$, $i \neq j$, actually evaluates the skew of the clock path delays with both NBTI and process variations considered.

3. Motivation for Controlling on Clock Path Degradation and Rate using Multi-V_{th} Clock Buffers

From Equation (15), it is clear that AS_{ti} evaluates the degradation sensitivity of the mean path delay considering NBTI effect. Since there are multiple buffers on a clock path,

AS_{ti} relates to the threshold voltages of all the buffers. Clock path delay is defined as the delay from the source clock to the sink D flip-flop. Assuming that clock paths m and n have same aging condition and structure, some buffers on path m are replaced with their high-V_{th} counterparts. From Equation (15), we can see that:

$$\mu_m(0) > \mu_n(0) \tag{20}$$
$$AS_{tim} < AS_{tin} \tag{21}$$

If the length of path m is sufficiently long, we can select multiple buffers to replace with their high-V_{th} counterparts, which could accumulatively decrease the degradation rate and successfully lead to $AS_{tim} \cdot \mu_m(0) < AS_{tin} \cdot \mu_n(0)$, where $\mu_m(0)$ and $\mu_n(0)$ are constants. By substituting it back to Equation (19), we can get:

$$\begin{aligned}\Delta\tau \leq\ & |\mu_m(0) - \mu_n(0)| \\ & -t^\gamma \times |AS_{tim} \cdot \mu_m(0) - AS_{tin} \cdot \mu_n(0)| \\ & +|\sqrt{\sigma_m^2(0) + \sigma_n^2(0) - 2\rho_{mn}\sigma_m(0)\sigma_n(0)}|\end{aligned} \tag{22}$$

It can be seen from Equation (22) that $\Delta\tau$ will decrease with time, as we replace sufficient number of buffers with their high-V_{th} counterparts on a path. It also indicates that by replacing multiple buffers on a path with high-V_{th} buffers, we can adjust its degradation rate with respect to another path. Figure 2 shows a simple illustrative example of two paths. By replacing two gates with their high-V_{th} counterparts, path 1 will have a higher initial delay at time 0; however, its degradation rate is decreased.

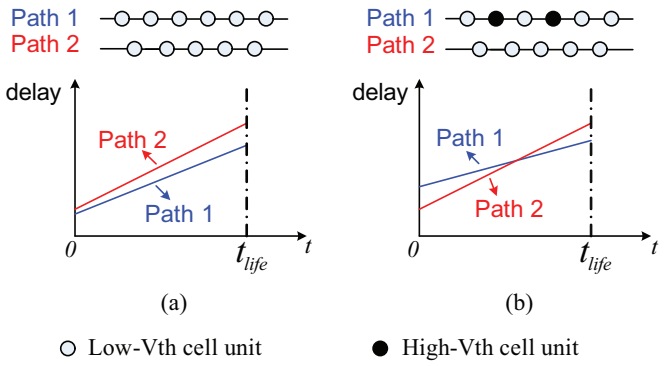


Fig. 2. Path delay and degradation comparison: (a) before replacement; (b) after replacement.

We can take advantage of this feature to reduce the clock skew induced by NBTI. However, we must also pay attention to the shift of clock path delay introduced by the buffer replacement. From Equation (22), gate replacement will lead to a new path delay with an upper bound as:

$$\begin{aligned}\tau_m(t) &= \tau_n(t) + \Delta\tau \\ &\leq \tau_n(t) + |\mu_m(0) - \mu_n(0)| \\ &\quad -t^\gamma \times |AS_{tim} \cdot \mu_m(0) - AS_{tin} \cdot \mu_n(0)| \\ &\quad +|\sqrt{\sigma_m^2(0) + \sigma_n^2(0) - 2\rho_{mn}\sigma_m(0)\sigma_n(0)}|\end{aligned} \tag{23}$$

If we compare the delays before and after replacement on the same path, obviously $\rho_{mn} = 1$. Thus, the upper bound of the path delay after replacement will be:

$$\begin{aligned}\tau_m(t) &= \tau_n(t) + \Delta\tau \\ &\leq \tau_n(t) + |\mu_m(t) - \mu_n(t)| \\ &\quad +|\sqrt{\sigma_m^2(0) + \sigma_n^2(0) - 2 \times 1 \times \sigma_m(0)\sigma_n(0)}| \\ &= \tau_n(t) + |\mu_m(t) - \mu_n(t)| + |\sigma_m(0) - \sigma_n(0)|\end{aligned} \tag{24}$$

If we have a timing constraint on the clock path delay: $\tau_n \leq \tau$, the new clock path delay after replacement should satisfy:

$$\tau_m(t) \leq \tau - \Delta\tau \tag{25}$$

Otherwise, the replacement will negatively impact manufacturing yield. Now, if we extend Equation (15) to include the process variations, it can be rewritten as:

$$\mu_{pv}(t) = \mu_{pv}(0)(1 + AS_{pv\_ti}t^\gamma) \tag{26}$$

Similarly, AS_{pv_ti} will decrease if some buffers on the clock path are replaced with their high-V_{th} counterparts. Assuming that the comprehensive timing analysis suggests that the worst delay value will become Γ at time t, a safety margin $\Delta\Gamma$ has to be assigned to the circuit at design time. Combined with the above analysis, the following constraint must be satisfied for a new replacement so as not to violate the design specification:

$$\Re = \begin{cases} 1 & \tau_m(0) \leq \Gamma - \Delta\Gamma - \Delta\tau, \\ 0 & Otherwise; \end{cases} \tag{27}$$

where $\tau_m(0)$ is the path delay at time 0 under nominal condition without process variations and NBTI impact. Here, we use the $\Re$ value as a flag to indicate whether a replacement is feasible when $\Re = 1$.

In summary, we can see that a new buffer replacement is optimal in reducing the clock skew only if the following requirements are satisfied:

$$\begin{cases} \tau_{after}(0) \leq \Gamma - \Delta\Gamma - \Delta\tau \\ SK_{after} < SK_{init} \end{cases} \tag{28}$$

where SK_{init} (SK_{after}) is the clock skew before (after) buffer replacement; $\tau_{after}(0)$ is the clock path delay at time 0 after replacement.

4. Clock Skew Reduction Flow

Our proposed synthesis flow for clock skew reduction is shown in Figure 3.

We use the PTM model to characterize the delay and degradation of the buffers in the standard cell library considering different V_{th} values. Thus, a multi-V_{th} clock buffer library can be characterized. In the physical design stage, clock tree structure can be obtained. Other NBTI-related parametric information can be collected using either commercial [23] or our in-house tools [24] [25]. Through an aging-aware timing analysis using the multi-V_{th} clock buffer library, the delay and degradation for the buffers and the clock paths are derived. Our clock buffer replacement algorithm make use of these information to identify the critical clock buffers (with standard-V_{th}) for replacement. The implementation of

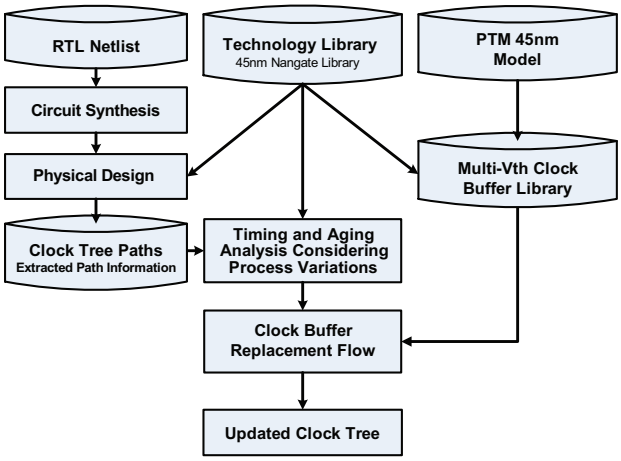


Fig. 3. Clock tree synthesis flow for skew reduction.

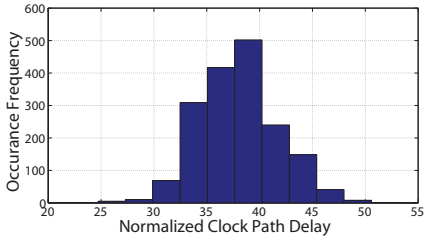
our flow will help reduce the clock skew with considering NBTI impact and process variations for a specified lifetime operation. The key step in our flow, namely clock buffer replacement, is described in Algorithm 1.

Algorithm 1 Clock Buffer Replacement

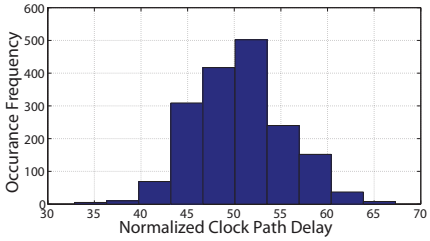
```
1: Extract X clock paths with L buffers from the clock tree
2: Obtain STA information of the X clock paths
3: Collect aging information of the X clock paths
4: Specify Δτ considering NBTI effect and process variations
5: Specify stress time t for NBTI aging analysis
6: Separate all the clock paths into N sets through buffer overlap analysis
7: for (All sets n from 1 to N) do
8:     for All paths m from 1 to M in current set do
9:         Select a clock buffer k from 1 to K on current path m
10:        if Buffer k is a non-overlap buffer by all the paths in set m then
11:            Evaluate the replacement using Equation (28) in current set
12:            if It is an optimal replacement then
13:                Replace the current buffer
14:            end if
15:            Update the timing information of the paths in current set n
16:        else if Buffer k is an overlapped buffer by all the paths in set n then
17:            Evaluate the optimality using Equation (28)
18:            if The replacement decreases the clock skew among buffer sets then
19:                Replace the current buffer
20:                Update the timing information of current buffer set
21:            end if
22:        end if
23:    end for
24: end for
```

In the algorithm, clock paths are separated into sets by analyzing the buffer overlap condition of the paths; paths in the same set will have high number of overlapped buffers. Aging information and lifetime specification for analysis are obtained from lines 1 to 5. We replace the non-overlapped buffers inside the current set to reduce clock skew from lines 10 to 15 while we select the overlapped buffers among sets from lines 16 to 23. Together, we identify all the necessary critical buffers to reduce the skew of the clock tree from lines 7 to 24. The computational complexity mainly comes from the optimality analysis for each clock buffer from lines 10 to 22. The overall computational complexity is $O(NMK^2)$, where N is the number of path sets, M is the average path count in a path set, and K is the average buffer number on a clock path.

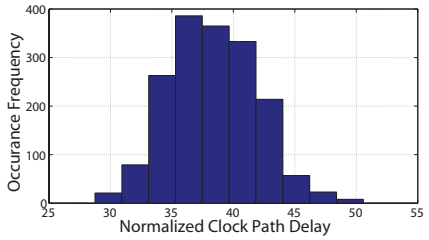
For a large-scale industry design, there would be an extremely large number of clock paths for analysis. To reduce the CPU runtime, one can use a "divide and conquer" approach. First, we divide the X clock paths into G groups, each of which has M/G clock paths. Second, we apply Algorithm 1 to each group. Accordingly, number of paths in each set decreases proportionally to N/G. Last, we apply Algorithm 1 to the groups to ensure any further skew optimization could be obtained. Thus, the complexity reduces from $O(NMK^2)$ to $O(NMK^2 \times \frac{1}{G^2})$, which is highly dependent on G. If we divide the overall X clock paths into a sufficiently large number of groups, the overall computational complexity will be substantially reduced.



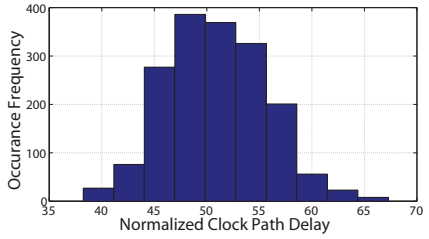
(a) Clock path delay distribution when $t = 0$ before buffer replacement



(b) Clock path delay distribution when $t = 10$ years before buffer replacement



(c) Clock path delay distribution when $t = 0$ after buffer replacement



(d) Clock path delay distribution when $t = 10$ years after buffer replacement

Fig. 4. Clock skew reduction for $ethernet$ benchmark circuit considering NBTI and process variation ($T = 125^oC$).

5. Results

In this section, we evaluate the effectiveness of our proposed flow. Five circuits from IWLS 2005 benchmark suite

TABLE I
CLOCK SKEW COMPARISON BEFORE AND AFTER BUFFER REPLACEMENT AT DIFFERENT STRESS TIME ($T = 125^oC$)

Bench. Circuit	Before Replacement				After Replacement				Skew Reduction (%)				
	$t = 0$ yrs	$t = 3$ yrs	$t = 6$ yrs	$t = 10$ yrs	$t = 0$ yrs	$t = 3$ yrs	$t = 6$ yrs	$t = 10$ yrs	$t = 0$ yrs	$t = 3$ yrs	$t = 6$ yrs	$t = 10$ yrs	Average
des_perf	14.37	18.26	18.73	19.12	9.20	13.40	14.13	14.72	35.98	26.62	24.56	23.01	27.54
ethernet	25.86	32.85	33.71	34.40	21.83	27.73	28.45	29.04	15.58	15.59	15.60	15.58	15.59
vga_lcd	44.60	56.67	58.14	59.34	35.42	46.75	49.72	50.96	20.58	17.50	16.21	14.12	17.10
netcard	40.33	51.23	52.57	53.65	27.61	38.60	41.71	42.89	31.54	24.65	20.66	20.06	24.23
leon3mp	43.56	55.34	56.79	57.95	37.34	47.44	48.67	49.68	14.28	14.28	14.96	14.27	14.45
									Average Skew Reduction (%)				≈ 20

are considered in our simulation. All the simulations are performed using open-source Nangate standard cell library with 45nm technology node [26]. PTM model and transistor parameter values [20] [22] are used to characterize the delay and degradation of the clock buffers in the cell library considering two V_{th} values. Compared to a standard threshold voltage of $0.28V$ by default, we set $0.45V$ as its corresponding high-V_{th} threshold voltage. The benchmark circuits are processed through the conventional ASIC design flow using Synopsys [23] and our in-house tools [24] [25] to extract the NBTI-related circuit information, e.g. clock tree structure, stress probabilities, etc.

Equation (28) explains that our flow reduces the clock skew by taking advantage of a previously specified safety margin value $\Delta\Gamma$. To avoid specifying an unnecessary safety margin, we modify the constraints in Equation (28) as follows:

$$\begin{cases} \tau_{after}(0) \leq \Gamma_{worst}(0) - \Delta\tau \\ SK_{after} < SK_{init} \end{cases} \tag{29}$$

where $\Gamma_{worst}(0)$ is the largest clock path delay without process variations and NBTI degradation at time 0. Compared with Equation (28), Equation (29) has a tighter constraint: only clock paths with a delay less than $\Gamma_{worst}(0)$ will be selected for the analysis on skew reduction. Results demonstrate that our flow still works efficiently under such an extremely constrained condition.

Figure 4 depicts the results on benchmark circuit $ethernet$. The clock path delay distributions at time 0 and 10 years are presented as a comparison before and after buffer replacement ($T = 125^oC$). Note that all the delay values in our presented results are normalized for the comparison purpose. The clock tree structure extracted from $ethernet$ is small in size and the clock paths are short in length (with an average length of $K = 8$ buffers on the clock paths). In total, $X = 1748$ clock paths with $L = 2524$ clock buffers are selected. Our flow identifies 11 buffers for replacement due to the short length and small size of the clock tree. Comparing Figures 4(a) with 4(c), the clock skew is reduced from 25.86 unit delay to 21.83 unit delay with a reduction of 15.58% at time 0. While considering 10 years of NBTI degradation, the clock skew is reduced from 34.40 unit delay in Figure 4(b) to 29.04 unit delay in Figure 4(d) with a reduction of 15.58% as well. Figure 5 presents the results on benchmark circuit $ethernet$ under five temperature scenarios: 25^oC, 50^oC, 75^oC, 100^oC, and 125^oC. After buffer replacement, the average clock skew reduction considering 10 years of NBTI degradation are plotted in the figure, which demonstrates that our methodology can effectively reduce clock skew under different temperature scenarios, i.e., benchmark circuit $ethernet$ can obtain around 15% skew reduction processed by our flow.

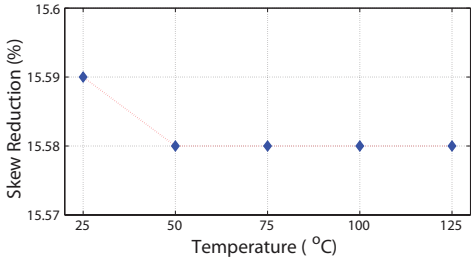


Fig. 5. Clock skew reduction for benchmark circuit $ethernet$ under different temperature scenarios.

TABLE II
CLOCK SKEW REDUCTION AND BUFFER REPLACEMENT ANALYSIS
($T = 125^oC, t = 10\ years$)

Bench. Circuit	# Paths (X)	# Buffers (L)	Ave. Path Length (K)	Overlap Freq. (F)	Buffer Replaced # Buffers	Buffer Replaced %	Skew Reduction (%)
des_perf	330	836	6	2.39	17	2.03	29.50
ethernet	1748	2524	8	5.54	11	0.44	15.58
vga_lcd	3068	6002	15	7.66	88	1.47	17.35
netcard	5455	6900	10	7.91	82	1.19	25.80
leon3mp	7955	9380	9	7.63	25	0.27	14.28
				Average		1.08	≈ 20

We also implement our flow on four other IWLS 2005 benchmark circuits des_perf, vga_lcd, $netcard$, and $leon3mp$. We compare the skew before and after buffer replacement at 4 different stress time instants: 0, 3, 6, and 10 years with the results shown in Table I under temperature $T = 125^oC$. Under the categories "Before Replacement" and "After Replacement", the clock skews corresponding to different stress times are listed. Correspondingly, the skew reduction and their average values are listed under the category "Skew Reduction (%)". Each row corresponds to one benchmark circuit. In the last row, the average skew reduction on these five benchmark circuits is calculated. Table I shows that our flow can effectively reduce the clock skew by around 20% on average under an over-constrained condition, considering 4 stress time points on these five benchmark circuits. Note that implementing our flow on large-scale industry designs with the constraint in Equation (28) should result in a much higher skew reduction, since all the clock paths will be equally analyzed, and all buffers will be evaluated for selection to further reduce skew.

We further analyze the relationship between the number of identified buffers and the skew reduction in Table II, where Columns 2 and 3 list the number of clock paths X and clock buffers L in each circuit. The average path length K for each benchmark circuit is listed in Column 4. The number of buffers identified for replacement and their corresponding ratio to the overall buffer count are listed in Columns 6 and 7. The last column shows the skew reduction for each circuit using our flow. Note that this value is an average of two skew

reduction values at time 0 and 10 years. We also calculate the "Overlap Frequency (F)" for each circuit in Column 5 as:

$$F = \frac{X \times K}{L} \tag{30}$$

where X is the total number of clock paths, K is the average path length, and L is the total number of buffers.

In Equation (30), the numerator calculates the necessary non-overlapped buffer count to construct the clock paths for a circuit, assuming that no two paths go through a same clock buffer. Thus, Equation (30) evaluates the average number of paths that go through a same buffer. It also indicates the average overlapped buffer count on each path. As discussed in Section 4, only replacing a non-overlapped buffer may reduce the delay difference between two paths. We can conclude that a higher F value indicates that fewer buffers are available for replacement, thus resulting in less skew reduction. For example, benchmark circuit des_perf has an average path length of 6 with an F of 2.39. On average, for each path in des_perf, it has more than 50% ($1 - \frac{2.39}{6} \geq 50\%$) of its buffers available for replacement. However, for benchmark circuit vga_lcd, it has less than 50% ($1 - \frac{7.66}{15} \leq 50\%$) of its buffers appropriate for replacement. Intuitively, the more buffers are available for replacement, the more clock skew reduction we can obtain. Also from our results, we find that the skew reduction is also highly dependent on the clock tree structure and clock path count. For example, to replace 88 out of 6002 buffers on the 3068 clock paths for benchmark circuit vga_lcd, we can obtain around 17.35% skew reduction considering 10 years of degradation. While a replacement of 17 out of 836 buffers on 330 paths for benchmark circuit des_perf can obtain 29.50% skew reduction. Furthermore, benchmark circuits $netcard$ and vga_lcd have relatively larger path lengths ($K = 10$, and 15) compared with the path lengths ($K = 8$, and 9) of $ethernet$ and $leon3mp$. The skew reductions on vga_lcd and $netcard$ are thus larger since more buffers can be selected for replacement, which renders our flow more favorable for large-scale industry designs with larger-length clock paths. Summarized from the results in Table II, our flow replaces only 1.08% of clock buffers and can obtain around 20% skew reduction under our over-constrained condition. One should also note that if an excessive number of buffers on the clock paths are replaced with the high-V_{th} buffers, the clock path delay may increase heavily more than the original one, deteriorating the speed of the circuit. In our flow, we also constrain clock path delay when reducing the skew as described in Equations (28) and (29).

In the replacement procedure, no additional transistors or gates are required. Thus, our flow incurs almost no area-overhead to the circuits. Another dominant concern in CMOS digital circuits is leakage current. As formulated in [27], this component exponentially decreases with the increase of the threshold voltage:

$$I_{Leak,k} \propto e^{\frac{q}{n\Lambda T}(V_{dd} - \gamma_1^{'} V_s - \gamma_2^{'} V_{DS} - V_{th})} \tag{31}$$

where q, Λ, V_s, $\gamma_1^{'}$, and $\gamma_1^{'}$ are the process or physical related constants. Considering the total leakage power $P_{Leak} = \sum_k I_{Leak,k} V_{dd}$ (k is the gate index), the replacement approach in our flow decreases the leakage power as well. The amount of leakage power reduction is proportional to the number of replaced buffers. Since our major optimization objective is to reduce the clock skew while maintaining the clock path delay within a range not violating the design specification, the buffers for replacement is optimized in the least number. However, our flow is still effective in reducing the leakage power. By combining the leakage power reduction into the optimization objective, we can replace more clock buffers to satisfy both skew and leakage power reduction. This is outside the scope of this paper.

6. Conclusions

In this paper, we propose an effective synthesis flow for clock skew reduction considering NBTI and process variations. Our flow takes advantage of the original safety margin, specified in conventional ASIC design flow. This margin is usually excessively large, that leads to significant performance loss. Our algorithm uses this margin to reduce the skew by identifying the critical clock buffers in the clock tree. These identified buffers are replaced by their high-V_{th} counterparts. Results show that our flow obtains high efficiency even under an extremely constrained condition. By introducing the "divide and conquer" approach, our flow is applicable to large-scale industry designs. In future, we plan to perform experiments on large industry designs to investigate the effectiveness of our proposed flow, as well as including leakage power in the optimization algorithm.

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