Identification of IR-drop Hot-spots in Defective Power Distribution Network Using TDF ATPG

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***Abstract*— As technology scales below 45nm and circuit integration density increases, power distribution network (PDN) contributes significantly to the total chip yield, escape, and reliability. Due to lack of controllability and observability, the PDN failure analysis has become extremely challenging. A robust PDN is essential to ensure the performance of circuits on-chip, especially for low power, high-speed designs. The area of PDN and the number of power vias and lines have dramatically increased in complex designs over the past several years resulting in increased defects on PDNs. In this paper, we present an efficient pattern generation flow that targets open defects on PDN. In this flow, the circuit layout is divided into smaller regions based on PDN structures. A vector-pair is generated to increase the region switching activity so that the gates will experience a larger-than-threshold IR-drop which may cause a timing or logic failure if only an open defect exists on power vias or power lines in that region. Various open defects on power/ground lines and vias are inserted and their impacts on circuit performance are investigated. A region sorting procedure is included in the proposed flow to reduce the computing effort. The proposed pattern generation and verification flow is implemented on ITC'99 benchmark circuit b19 and experimental results on open defect-induced IR-drop is presented and analyzed in this paper.**

Keywords: Power Distribution Network, Open Defect, ATPG, IR-drop

I. Introduction

The power distribution network (PDN) delivers power and ground voltages from pads in a wire-bond package or C4 bumps in a flip-chip package to all cells on the chip. A robust power distribution network is essential to ensure correct and reliable operations of modern high performance VLSI circuits. As technology scales, designs are becoming increasingly sensitive to power supply noise. Power supply noise refers to the noise on power and ground distribution network, which reduces effective power supply voltage levels reaching gates. High average currents cause large ohmic IR voltage drop [1] and the current transients cause large inductive Ldi/dt ground bounce [2] in the power distribution networks [3]. The main effects of IR-drop and ground bounce are on circuit timing and signal integrity. Since power supply reduction will slow down the gate transition, IR-drop and ground bounce affects setup and hold times as well as clock skew [4] which will result in silicon failure. Experiments show that a 2.4x increase in gate delay can be observed during simulation with a 12.5% decrease in supply voltage at a 130nm technology node [5]. The power distribution network must be designed to minimize these voltage drops and maintain the local supply voltage within specified noise margins.

As functional clock frequency and gate density increase, the simultaneous switching activity of the chip will also increase. This will result in a higher peak and average current concentrated in areas of the chip with higher gate density, stressing the PDN that is supplying that area. A large amount of power has to be distributed to all the gates and devices across the entire chip through a hierarchy of up to ten metal layers. This trend creates a big challenge for power distribution network design and testing [6]. Different from logic cells, power/ground vias and lines are not accessible by primary inputs or scan flip-flops. Due to the complexity of the PDN and lack of controllability and observability, it is extremely difficult to deal with PDN manufacturing defects. The PDN reliability challenges caused by technology scaling have been discussed in [7]. It is a common practice to use 20% to 40% of the metal resources to build a high density PDN in modern high performance microprocessors [8] [9]. Since the PDN utilizes such a large portion of area in a design, from inductive fault analysis [10], the probability of defects occurring on its vias and interconnects can be quite high, especially considering that the width of modern PDNs are only 2-3X the width of interconnects.

There is a fundamental difference between gate defect and PDN defect behavior in the circuit. A gate defect can cause a gate malfunction or impact the circuit function or timing behavior. A PDN defect, however, may not necessarily result in functional failure. Contrary to the common assumption that defects on PDN can be detected by implication during functional or structural test, only a small percentage of such defects that result in catastrophic failure can be easily detected during manufacturing test. Defects on PDNs could cause (1) reliability problem that passes the functional test and cause an in-field failure and (2) functional failure that could be detected during manufacturing test. Although, our goal in this paper is to generate patterns to detect open and resistive opens on PDNs, the patterns are most useful during pre-tapeout steps of design process where the PDN robustness can be verified. By applying such patterns, the designers would be able to redesign the PDN by inserting additional vias or power wire sizing and eliminate the impact of a defect if exists after fabrication resulting in reduced escape and increased yield. Since defects on power/ground vias and power wires adversely affect yield in addition to severely impacting reliability, time-to-market and profitability, there is a need to detect these defects and identify their location on the PDN for a better design-for-manufacturability (DFM).

A procedure called box-scan search which identifies possible weaknesses in a power distribution network of an LSI is proposed in [11]. By scanning the node voltages of the virtual box, a prioritized list of weak points which must be fixed is generated. Due to the high computing complexity, this vectorless method is not suitable to modern VLSI circuits with hundreds of millions of nodes. Also, this method only considers vias omitted from the design during the PDN design phase rather than manufacturing defects. A via distribution model for yield estimation is developed in [12]. It presents the relationship between failure rate, number of vias, and the yield. A distinction between signal vias and vias on the PDN was not made.

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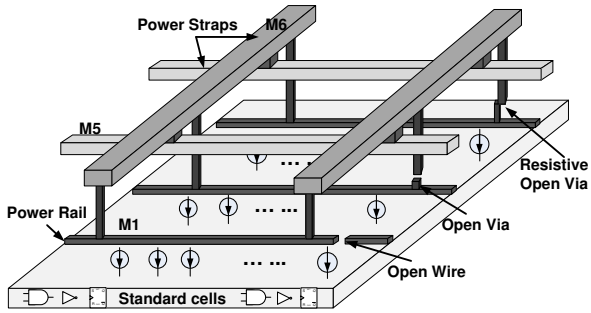

Fig. 1. A representation of power/ground distribution network and potential open defects.

However, since vias on the PDN supplies current to multiple cells, not having enough vias on the PDN may starve multiple cells in a surrounding region and cause failure. Therefore, insufficient vias on the PDN may have a higher negative impact on yield than insufficient vias on signal lines. Accordingly, if defects were to cause a situation where there was insufficient current to flow to multiple cells, there would be a larger, likely undetectable, impact on the chip.

The contributions this paper makes are:

- We propose a new pattern generation procedure to target open/resistive open defects on PDN vias and wires.
- Since there is a very large number of PDN wires and vias, we will identify non-robust regions of the PDN that are highly susceptible to timing or functional failures in presence of open defects. This procedure significantly reduces the number of regions to be targeted thus reducing the CPU run-time considerably.
- A novel layout-aware pattern generation procedure is developed to target these regions to determine the presence and impact of open/resistive-open defects.
- Large IR-drop caused by our generated patterns and physical defects are investigated and their impact on circuit function and timing is analyzed.
- Finally, we present a few recommendations for avoiding hot-spots and timing failures induced by defects on PDN.

The paper is organized as follows. Section II describes PDN failure analysis. The pattern generation flow is presented in Section III. To demonstrate the effectiveness of the proposed pattern generation procedure in detecting open defects, we implement this method on ITC'99 [16] benchmark circuit b19 in Section IV and the results are shown. Finally, concluding remarks will be given in Section V.

II. PDN Failure Analysis

A. PDN Structures

Power and ground distribution networks are typically designed hierarchically, from block level to chip level. The block level PDN, which is also called local PDN, is designed either in a fully customized way (usually for hard blocks) or using an automated router to uniformly arrange the power/ground over standard cells. In high performance digital ICs, a grid structured network is widely used for global PDN design, while the structure for local PDN can be different from block to block. In a typical integrated circuit, the lower the metal layer, the smaller the width and pitch of the lines [13]. Comparing with global PDNs which are routed on higher metal layers with wider lines and redundant vias, local PDNs are more prone to be affected by spot defects, process variations, and electromigration. In state-of-the-art SOC circuits, such as microprocessors, hundreds of millions of power/ground vias and wires are used to deliver power and ground to all cells. Consider a uniform distribution of the spot defects, according to inductive fault analysis (IFA), proposed in [10], area intensive routing, such as local PDNs, will result in more defects. As technology scales, more open/resistive-open vias and wires are expected to occur on local PDN. Due to characteristics and little or no accessibility, it is difficult to locate the PDN defects before tape-out or after the chip is fabricated and tested.

To further clarify the objective of this work, in this section, we use a grid structured PDN as shown in Figure 1 as an example, to analyze the impact of possible open defects on the circuit performance and functionality. Such grid structured network is used for designing the PDN for b19 benchmark during our experiments.

In the power distribution network shown in Figure 1, vertical power straps on Metal 6 and horizontal power straps on Metal 5 build up a grid structured network which can distribute power/ground across the entire chip. The lowest level power/ground (P/G) lines on Metal 1 run horizontally as power rails. Standard cells are arranged in rows and connected to Metal 1 P/G wires with two adjacent rows sharing the same power line. Each P/G rail in Metal 1 is connected by vias to the P/G lines in Metal 6 at the overlap sites, respectively. Metal 1 connects to the Metal 6 PDN through stacked vias. Open/resistive-open defects on power wires and vias have also been shown in Figure 1 and will be discussed in the following sub-section.

Since significantly wider wires are used in global PDN, the probability of an open defect is extremely low. In this work, we only focus on defects on the local PDN, which is Metal 1 power rails in our b19 benchmark design. At this level, the power line width is about 2x that of circuit interconnects connecting logic cells, power/ground vias connecting logic cells to power/ground lines, as well as vias connecting the upper-metal layers to power lines in Metal 1. Note that in a stacked via, the via connecting to Metal 1 is the smallest, which is less than a quarter of the power line width. Note that, we will use term "PDN" for "local PDN" in the following sections.

B. Open Defects on PDN

While power lines tend to exhibit similar defects as any other interconnect in a design, the impact of these defects on the circuit depends on the power grid design. However, most defects in various PDNs will result in similar faulty behavior. As an example, an open defect on the power line or power via will weaken the power network and result in an increased IR-drop, changes in delays in the neighboring cells, and possibly multi-path delay faults. If one of multiple redundant power vias from an upper-layer metal to a lower-layer metal is broken, the network is still connected, but weakened. As a result, the PDN will not be able to supply as much power to the underlying cells potentially causing timing and functional failure if the current demand for that region becomes too high. Similar behavior may result from shorted vias and shorted power line defects. For instance, a local drop in voltage will occur around the short, but farther away there may be no perceptible difference.

In this work we will only consider open defects on the PDN and we will address the issue of resistive opens in PDNs in future work. In Figure 2, an open via defect with its two nearby regions is shown. With the open via defect existing, gates underneath the open via (region 2) cannot draw current through via in that region (region 2) from the upper-layer PDN. The cells in region 2 will likely draw current from neighboring vias, vias in regions 1 and 3 as shown with arrows in Figure 2. This will increase the current flowing through the power vias and wires in the two neighboring regions, and thus will cause increased IR-drop in neighboring regions. For the cells in the region with open via, since they need to draw current from further power vias, their power pin resistance increases and thus also suffer

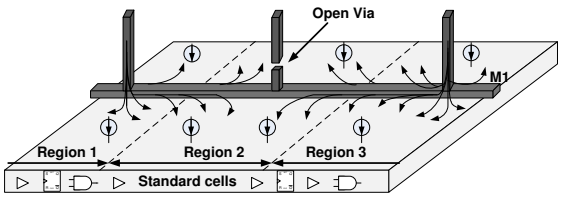

Fig. 2. Open Via defect on Metal 1 power line.

from increased IR-drop. As for open wire defect, in the region with open defect, only cells that are separated from the nearest power vias will see IR-drop increase. Cells in the neighboring region of one side of the open defect will suffer from increased IR-drop as well due to the increased current drawing through their Metal 1 power rail. Such increased IR-drop in neighboring regions due to open defect may result in functional or timing failures, especially when there is already a large amount of switching activity in any of the neighboring regions (region 1 or region 3).

In case of resistive opens on vias or P/G wires, the increased R will increase IR-drop in the region where the defect exists, i.e. similar behavior as expected. Therefore, the method developed in this paper should detect these types of defects as well.

III. Pattern Generation Procedure

To address the above issues, test patterns must be generated to target and detect the open defects in the PDN since relying on incidental detection may negatively impact reliability and escape. As shown in Figure 3, the proposed procedure consists of three major steps: *(1)* Region sorting; *(2)* Pattern generation; and *(3)* Pattern validation. After the physical design, the post-layout netlist file and the DEF (Design Exchange Format) file will be generated. The DEF file which contains physical placement information of the elements in the circuit will be used to define regions in Step 1.

A. Step 1: Region Sorting

Since there are numerous vias on power/ground rails in Metal 1, targeting all vias and interconnects would be too time consuming and impractical. To increase the processing speed and reduce the calculation effort, regions are targeted rather than individual vias. This will allow a single pattern to detect many potential open defects at one time. Since some regions of the chip are more susceptible to IR-drop issues created by opens than others, a region sorting method is proposed and integrated into the pattern generation procedure to further reduce the CPU run time.

The design is divided into regions based on the upper-layer PDN structure, which was generated during physical synthesis. For a chip with a rectangular power ring and *k* vertical and *l* horizontal power straps, the design is divided based on the intersection of the straps/rings as midpoints for each region in the matrix which is similar to power pads in very large designs. This will create a matrix with $m = (k + 2)$ columns and $n = (l + 2)$ rows for a total of $m \times n$ regions as shown in Figure 4. Each region of the matrix maps directly to a region in the layout. In order to identify those regions that are most vulnerable to open defects, *maximum weighted switching activity* (WSA_{max}) [14] is calculated for each region to profile the layout.

The maximum weighted switching activity (WSA_{max}) for region (*i,j*) is calculated with Equation 1 [14].

$$WSA_{max_{ij}} = \sum_{k=1}^{Ng(i,j)} (\tau_k + \phi_k f_k) \quad (1)$$

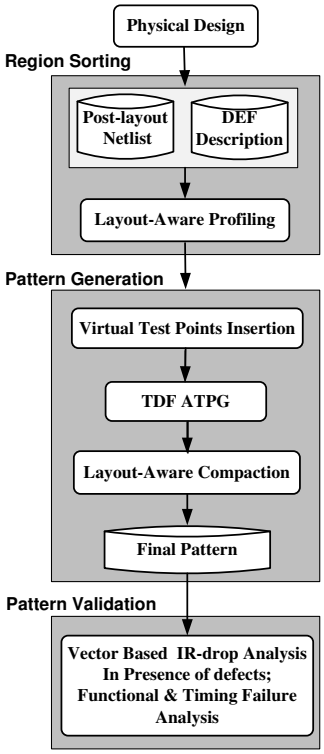

Fig. 3. Pattern generation flow for open defects detection on PDNs

where $Ng(i, j)$ denotes the total number of gates in region (i, j). WSA_{max} for region (i, j) is determined by the weight of a switching gate, τ_k, the number of fan-out of each gate, f_k, and the fan-out load weight, ϕ_k. After profiling the chip using WSA_{max}, the regions are sorted based on the total sum of three adjacent regions, $WSA_{max\_sum_{ij}}$, as calculated in Equation 2.

$$WSA_{max\_sum_{ij}} = WSA_{max_{(i-1)j}} + WSA_{max_{ij}} + WSA_{max_{(i+1)j}} \quad (2)$$

Note that three adjacent regions are considered for calculating $WSA_{max\_sum_{ij}}$, considering the middle region to be the target region and the other two as regions being impacted in case of the open defects (see Figure 2).

To limit the total number of regions targeted, we set a threshold WSA_{max_thr} based on the average functional WSA and then select regions with higher-than-threshold WSA_{max}. In this way, those regions that will not experience a significant IR-drop even in the presence of a single open or resistive open defect on the power vias/lines can be filtered out. Therefore, all regions with greater than WSA_{max_thr} could be targeted for open defects and regions under the threshold will be omitted.

B. Step 2: Pattern Generation

In the second step of the procedure, the goal is to generate a pattern that can exacerbate any defects present in the local PDN. To highlight these defects, patterns will be generated that introduce large switching activity both in the faulty-via centered region (region 2 in Figure 2) and the two adjacent regions (regions 1 & 3 in Figure 2). By increasing switching activity in all three regions, after applying test patterns generated by our procedure, the open/resistive-open defects

on local PDN that make the PDN non-robust can be detected by observing the timing failure of the chip under test.

To maximize the switching activity in the selected three regions, transition delay fault (TDF) ATPG is used. Note that the switching will increase as much that will still be below the threshold which is the average functional switching set by designer during power distribution synthesis step. The term "Maximize" is used in this paper but it is intended to show that the switching is increased but still stays below threshold.

To generate patterns with greater switching in the target region, two steps are taken: (1) All the flip-flops in the three regions are considered as observation points during TDF pattern generation; (2) Virtual test points are inserted at the output of gates in these three targeted regions. Outputs of all gates in the three regions are considered as fault sites. The virtual test points provide new observation points to (i) reduce the amount of effort the ATPG needs to propagate the transition to an observation point, (ii) increase the number of transitions, and (iii) reduce the number of care-bits in the pattern when generating one pattern per fault site.

The new netlist, called temporary netlist, with virtual test points inserted is used during ATPG for pattern generation in our proposed procedure which is briefly described in the following.

This method generates one pattern using TDF ATPG for each fault site in the selected regions. The procedure treats each net as a fault site. In this case, p vectors will be generated, where p is the total number of ATPG testable TDF fault sites in the targeted regions. These patterns are then compacted using a layout-aware compaction algorithm to generate a single patten for the target regions. The employed compaction algorithm will count the switching activity in the selected region introduced by each vector and only compact those vectors that will increase the switching activity in the targeted regions. Once the switching activity of the compacted pattern has reached the user-defined upper threshold, the compaction program will stop compacting the vectors. The compaction is a simple greedy algorithm that checks the bit-compatibility of each two consecutive vectors in the vector set and compact them.

Note that we use launch-off-capture (LOC) method to generate TDF patterns using ATPG therefore, with a very high probability, our generated patterns are functionally valid.

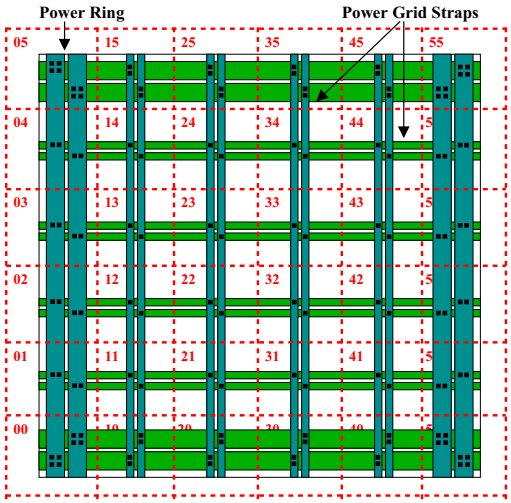

Fig. 4. An example of the region division based on the location of PDN straps.

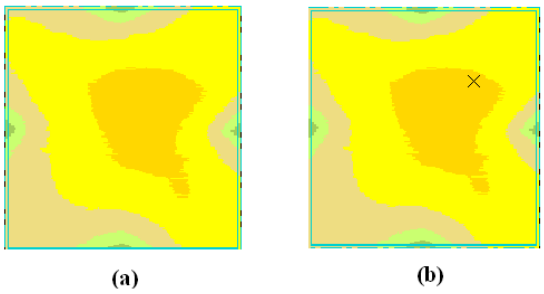

Fig. 5. IR-drop plot with a TDF random filled pattern for (a) fault-free circuit; and (b) circuit with open power via defect.

C. Step 3: Pattern Validation

In order to validate the effectiveness of the generated pattern in Step 2, we intentionally create an open via (we have tried open wire as well) on the PDN in the targeted region. In the presence of an open defect, a large amount of current will be drawn from neighboring vias. If the total current drawn from power vias in the neighboring regions (e.g. regions 1 and 3 in Figure 2) is greater than the threshold, it will likely result in a timing (if the path is going through these three regions is critical) or functional failure (if voltage drop on a gate in these regions is very large) during test. If the chip fails, then the targeted region is identified to have open defect; if the chip still works properly, then the PDN is considered as robust even in presence of open defects. This robust property also implies that such via is redundant in the design and can potentially be removed to save area. A simple way to do the pattern validation is to compare the worst IR-drop with and without open defects in the selected regions. The pattern generated in Step 2 will be used as input vector and vector-based IR-drop analysis will be conducted.

To evaluate whether the single pattern can target all the possible open defects in the selected region, we create a single open defect at different locations throughout the targeted region. This will verify the effectiveness of our pattern with respect to all the possible open defect sites in the targeted region. The defect will be moved in two different directions through the region, which are along the vertical axis perpendicular to the Metal 1 supply rails and along the horizontal axis on the same Metal 1 supply rail.

To evaluate the impact of IR-drop hot-spots created by the non-robust local PDN on timing performance, we will perform IR-drop aware timing analysis based on the vector based IR-drop analysis results. We expect that the degrade on supply voltage because of the defective open on PDN can result timing failure or functional failure.

IV. Experimental Results

To verify the proposed open defect detection method, we use ITC'99 benchmark b19 for our case study. The physical synthesis is performed using a 180-nm technology with 1.8 V supply voltage. Region definition and layout-aware profiling using WSA_{max} matrix were developed in C program and integrated into the Verilog Programming Language Interface (PLI). The chip level PDN in this design consists one core ring around the core boundary together with 10 groups of power straps in the vertical and horizontal direction, respectively. Overall 121 regions are defined for this benchmark. One pair of power/ground pads per side is used in this design. The regions are defined in the following sequence: the region in the most left bottom corner is numbered as region (0, 0) and the most right top one is region (10, 10). By running the region sorting program, region (7, 7) is selected as the targeted region for pattern generation since

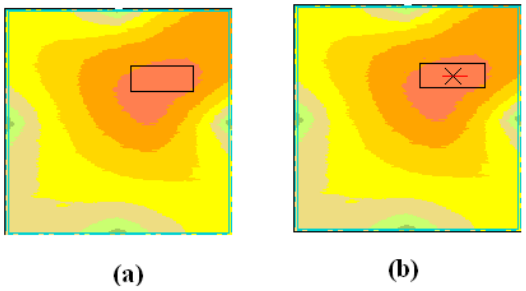

Fig. 6. IR-drop plot with pattern generated by our method for (a) fault-free circuit; and (b) circuit with open power via defect; rectangle highlights the selected 3 regions.

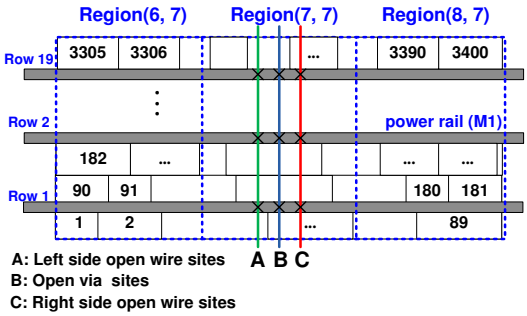

Fig. 7. Cell location in the selected 3 regions and the open defect sites used for verification.

the sum of WSA_{max} value of region (7, 7) and its two neighboring region, region (6,7) and region (8, 7) was greater than WSA_{max_thr}.

Figure 5 presents the IR-drop plot for fault-free circuit and circuit with an open via defect using a random-filled TDF pattern targeting faults in region (7, 7). For the IR-drop plot with open defect, there is no color difference at the fault site. Thus we know the increased IR-drop value should be less than 25 mV (one color represents an IR-drop voltage range of 25 mV). Because of the low switching activity at the fault site, the increased IR-drop is not large enough to cause a timing failure or logic failure since the IR-drop value is still within threshold. In this way, the TDF pattern will not detect the open defect and incorrectly classify this faulty PDN as a robust design, which is in fact non-robust. Similar IR-drop values were obtained from a large number of random TDF patterns targeting faults in region (7, 7). The average IR-drop in region (7, 7) caused by those TDF patterns is 94.7 mV, while the pattern generated by our method has an average IR-drop of 129.6 mV in region (7, 7). Figure 6 shows the IR-drop plot for the fault-free circuit and circuit with an open via with the pattern generated using our method. In this figure, the IR-drop value at the fault site has exceeded the pre-defined threshold, which greatly increases the chance for this open defect to be detected by observing timing failure during test if any of the gates affected by such large IR-drop are part of a long or critical path.

To illustrate the impact of open defects with respect to location, we create an open via defect as well as two open wire defects, one at the left side and the other on the right side of the center power via. According to our defect analysis in Section II, when gates in the specific region cannot draw current through their nearest via from the upper-layer PDN due to the open defect, they will draw current from vias in the neighboring regions. Therefore, IR-drop increases in both the target region with open defects and its neighboring regions.

Figure 7 shows the arrangement of the cells in the targeted region and its adjacent regions. Starting from the bottom left corner, cell numbering will increase from left to right and from bottom to top across all three regions. This numbering system will be used to identify the cells' individual IR-drop. Figure 7 also demonstrates the sites of the three open defects' movement along the vertical axis which was used for validation.

The IR-drop curves in Figure 8 show the IR-drop increase along a single Metal 1 power rail with an open via, open wire at left side and right side of the center power via. The x-axis shows the cell location number as described in Figure 7 and the y-axis represents IR-drop increase. Between the three defects, the open via defect has caused a significant IR-drop increase on both sides. While an open power wire defect only caused an IR-drop increase to one side of the defect since those gates have to draw current from the via in region

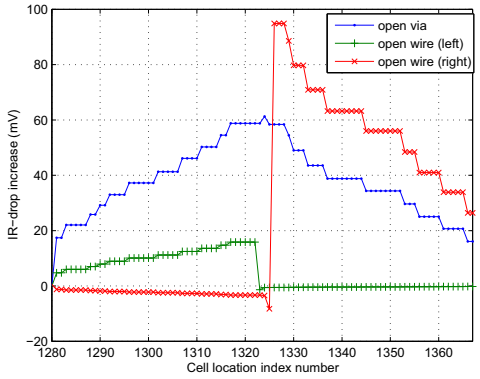

Fig. 8. The increased cells IR-drop value in row 8 for different open defect; the x-axis number represents the cells location in this row across three regions with smallest number (1280) at the left end and largest number (1369) at the right end of this row; defects are inserted between cell 1322 and 1325;

(7, 7). From Figure 8 we can also see that the cells on the right side of central via have larger current drawing ability. When open occurs and they cannot draw current from the nearest power via, those cells suffer a larger IR-drop increase.

Figure 9 presents the value of the IR-drop increase for all the cells in the targeted regions with each curve representing a single open wire on one of the 19 different power rails in the same x-coordinate. In this figure, the cell location number shown in Figure 7 is used as the x-axis. So, as the open defect moves from one power rail to the next rail, the maximum IR-drop for each row will vary depending on the number of switching gates and its respective load. Since each supply rail is shared between two rows an open defect will cause both rows to experience an IR-drop increase, which explains the reason for two peaks per open wire defect.

Table I summarizes the peak voltage drop in each row in the targeted 3 regions induced by the pattern generated using our method and the increase in IR-drop due to open defects on each power rail with our pattern applied. Three different types of open defects have been investigated, which are open via, open wire at the left side of the central power via (left-open) and open wire at the right side of the central power via (right-open). Column 2 is the peak IR-drop value in each row caused by this pattern in a fault-free circuit; Here the voltage drop numbers are calculated over a shortened period (2ns) within one clock cycle (8ns) where most of the switching happens. So the IR-drop here is a dynamic voltage drop value which reflects the supply voltage drop caused by the simultaneous switching. Columns 3-5 show the additional IR-drop increase over the one induced by the pattern. Column 3 shows the maximum IR-drop increase in each row

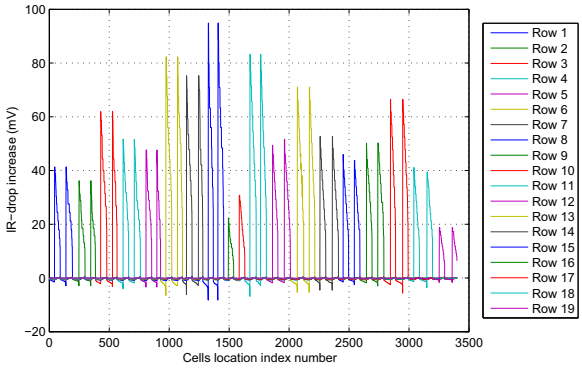

Fig. 9. The increased cells IR-drop value with right side open wire defects occurring on different supply rails.

due to the left side open wire defects in the targeted region; Column 4 presents results for open via defects; Column 5 generates results for the right side open wire defects. From the results we know that in the three selected regions, the cells on the right side have a larger current need and thus a right side open wire defect causes larger IR-drop increase. In this case, the right side open wire defect has more negative impact on the cells.

To make the PDN more robust for this region, adding an extra power straps between region (7, 7) and region (8, 7) is one solution. Comparing with the right side, the PDN design for the left side cells is more robust. Only rows 1 8 have significant IR-drop increase. To avoid the open wire defect failure in this region, we can redesign the PDN using wider power rails for those rows. To avoid the open via defect failure, redundant vias can be inserted as a backup power via to make the PDN more robust.

To demonstrate the impact of open-defect induced IR-drop increase on timing, we choose one flip-flop from row 8, which has a cell delay of 0.601 ns in a fault-free circuit, 58.37 mV and 94.87 mV IR-drop increase for open via and right-side open wire defect, respectively. By running IR-drop aware timing analysis, we observed that its cell delay increased by 30 ps and 48 ps, respectively, for the two kinds of open defects. If more cells along the critical path have been affected by open defects, the cumulative delay would be significant enough to cause a timing failure in a delay test. The exessive voltage drop on a gate could also cause a functional failure and degrade the reliability. For designs in advanced technology, like 90nm or 45nm, the IR-drop derating factor is even larger and thus same IR-drop increase will cause a much larger cell delay. In this way, designs in advanced technology will be more sensitive to PDN open defects.

V. Conclusion

In this paper, we have presented a novel pattern generation procedure for PDN open defect detection. The impact of open defects on vias and Metal 1 supply rails have been analyzed. A WSA_{max} based region sorting procedure has been used in the proposed flow to reduce computing effort. A pattern generation method has been proposed and included in the flow to create switching in those regions susceptible to the open defects. IR-drop analysis was performed with open defect inserted throughout regions that were suspected having non-robust PDN. By increasing the switching activity in the region with an open defect and its neighboring regions, the faulty rail can be potentially detected by observing any possible timing failure or logic failure using delay test.

TABLE I

IR-drop analysis with pattern generated using our proposed procedure for *b19* benchmark.

Row #	IR-drop induced by our pattern (mV)	Increase in IR-drop due to open defects (mV)		
		left-open	open via	right-open
1	198	42.53	48.41	41.31
2	201	**47.14**	48.00	36.23
3	202	31.72	51.92	61.92
4	201	22.10	45.07	51.72
5	201	20.60	41.81	47.64
6	212	18.69	56.53	82.29
7	205	6.107	47.55	75.30
8	211	15.84	**61.26**	**94.87**
9	191	0.68	7.44	22.37
10	192	1.07	42.59	30.75
11	210	0.05	20.85	83.24
12	198	0.65	29.65	51.60
13	203	1.69	21.05	71.03
14	201	0.89	15.93	52.63
15	193	0.49	19.25	45.97
16	191	1.18	9.10	50.22
17	196	1.14	26.74	66.50
18	187	1.41	13.09	41.13
19	184	1.16	2.823	18.81

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