TSUNAMI: A Light-Weight On-Chip Structure for Measuring Timing Uncertainty Induced by Noise During Functional and Test Operations

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ABSTRACT

Noise such as voltage drop and temperature in integrated circuits can cause significant performance variation and even functional failure in lower technology nodes. In this paper, we propose a light-weight on-chip sensor that measures timing uncertainty induced by noise during functional and test operations. The proposed on-chip structure facilitates speed characterization under various workloads and test conditions. Simulation results show that it offers very high sensitivity to noise even under variations. The structure requires negligible area in the chip.

Categories and Subject Descriptors

B.8.1 [**Performance and Reliability**]: Reliability, Testing, and Fault-Tolerance

Keywords

Power supply noise, Temperature, On-chip measurement, Speed characterization, Post-silicon validation

1. INTRODUCTION

Over the past four decades, technology scaling has greatly improved performance and circuit integration density. However, integrated circuits (IC) performance has become less predictable by simulation at design stage due to process and environmental (temperature, crosstalk, and supply voltage noise) variations. As a result, performance limiters, such as noise in the circuit, need to be identified as early as possible during first silicon test and debug and when performing speed characterization during manufacturing test [1][4][5].

Power supply noise (PSN) and temperature's impact on functional operation of the chip as well as test has been extensively investigated in the past several years [1]−[8]. Power supply noise and temperature have shown to have both local and global effects on circuit timing [2][5]. An excessive drop in the power supply voltage can cause a temporary malfunction in the circuit. Additionally, excessive noise could result in miss-binning of the chip under test.

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It is beneficial, from design timing stand-point, to measure the noise in post-silicon in functional mode to perform appropriate margining and supply voltage and frequency calibration using adaptive techniques [17]. Understanding the impact of supply noise on circuit timing can also help better correlate structural tests with functional tests for timing characterization and speed binning [9][10].

On-chip measurement architectures have gained significant attention in recent years [11]−[16] to be embedded in the chip for rapid first silicon test, debug, speed characterization, timing margining, IR-drop and temperature measurement, and wear-out mechanism analysis, for which all cause timing uncertainty in the device under test. Such architectures can help record the operation condition in the test mode as well as in the field and help perform post-silicon calibration [3][12][13]. For instance, the authors in [12] proposed SKITTER, an on-chip measurement circuit, to measure timing uncertainty from combined sources in the circuit. Although very effective in capturing noise effects, it requires large area overhead. The on-chip droop detector (ODDD) system designed in [13] enables voltage transient detection as well as a capability to induce voltage transients in a controlled manner to test and debug. The architecture is capable of measuring low frequency noise very accurately in the circuit however it will not be able to measure high frequency voltage noise as effectively, e.g., during launch-to-capture cycle in delay test schemes.

In this paper, we propose a low-cost and light-weight on-chip structure called SUpply Noise- and Temperature-Aware Timing Measurement Instrument (TSUNAMI), taking into account combined effect of supply noise and temperature on clock and on a reconfigurable delay line, to accurately measure the induced timing uncertainty even under process variations. TSUNAMI requires very low area overhead but provides high resolution and sensitivity to voltage noise, especially as technology scales. TSUNAMI consists of two major parts namely: (1) PSN sensor that is based on a reconfigurable delay line, and (2) A control vector unit that configures the PSN sensor and controls the measurement process. Both require negligible area on the chip.

TSUNAMI can operate in both test mode and functional mode. In functional mode, it can measure timing uncertainty (i) during every clock cycle of interest and (ii) within a clock cycle when applying the functional workload. The change in the timing information of the PSN sensor can be converted to the actual noise (e.g., power supply noise) information. In test mode, TSUNAMI can help measure voltage noise during scan as well as launch-to-capture cycle. In addition, it can help measure the noise level depending on the applied launch cycle to analyze the impact of Ldi/dt during

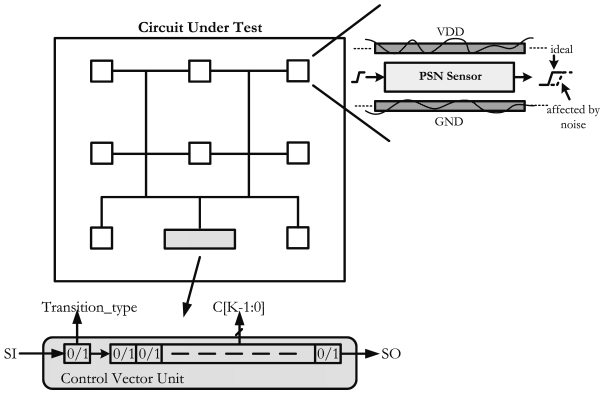

Figure 1: TSUNAMI architecture.

launch-to-capture cycle. Note that, although we call our sensor a PSN sensor, it is in fact able to capture combined timing uncertainty induced by both power supply noise (voltage drop and ground bounce) and temperature in every clock cycle.

The rest of the paper is organized as follows. In Section 2, we introduce the proposed TSUNAMI architecture. Calibration of TSUNAMI is discussed in Section 3. Section 4 presents problem modeling and design flow of TSUNAMI, and Section 5 presents simulation results and analysis. Finally, Section 6 concludes the paper.

2. TSUNAMI ARCHITECTURE

Today's modern designs include very large power distribution network. The voltage noise distribution in the design is not uniform as different blocks in the chip switch differently. Therefore, to take a snapshot of voltage noise distribution in the circuit, we need to insert sensors and measure the noise at various locations of interest under different workloads and test conditions. For instance, one area of interest for sensor insertion is near critical paths. The information can then be analyzed for characterization during post-silicon test, debug, and calibration.

The architecture of TSUNAMI, shown in Fig. 1, consists of PSN sensors, which are distributed across the layout to capture noise at different locations, and a control vector unit, which controls all the sensors.

Transitions are generated at the input of the PSN sensor and propagated through its components. The arrival time and slew of the transitions are affected by the noise on the power/ground lines generated by circuit switching. The PSN sensor is designed to be sensitive to noise. For the sensor to capture noise, it is preferred to be designed as a single macro and placed between power and ground lines. The noise on the power/ground lines will impact the transition propagation time (since it impacts gates' delay in the sensor). The impact of noise can therefore be observed as an additional delay.

Figure 2 shows the detailed implementation of the PSN sensor which consists of the following components: (1) a reconfigurable delay line (RDL), (2) a transition generation (TG) cell, and (3) a transition capture (TC) cell.

1. Reconfigurable Delay Line (RDL): RDL is composed of K reconfigurable stages in addition to an extra fixed stage; each reconfigurable stage contains a multiplexer choosing from an input branch with/without buffer, thereby providing different delay values, while the fixed stage is a series of buffers providing an additional delay that increases beyond what the K reconfigurable stages provide without

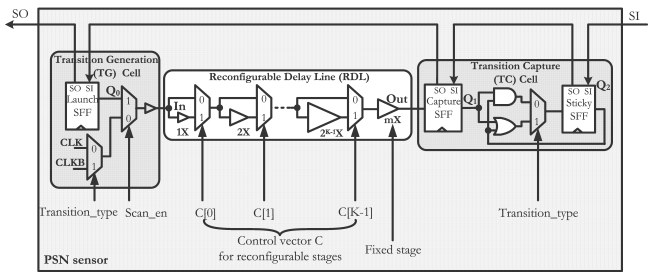

Figure 2: Our proposed PSN sensor.

introducing an additional reconfigurable stage. Thus, by controlling the select signals $C[0]$, $C[1]$, ..., $C[K-1]$, the delay of the entire line becomes reconfigurable. Furthermore, delay of the buffer at each stage is twice the buffer delay in the previous stage. Thus, if each MUX has a delay of t_x and the minimum-sized buffer has a delay of t_b, the minimum and maximum delay that RDL can provide are t_{min_RDL}=$K * t_x + m * t_b$ and t_{max_RDL}=$K * t_x + (2^K - 1 + m) * t_b$, respectively. Since the PSN sensor is designed as a single module, the interconnect delay between the sensor's components is considered negligible.

Different C values create different paths between the input (In) and output (Out) of the RDL. When C="00....00"=0, the path only includes the MUXes, making it the shortest path. However, when C="00....01"=1, the path goes through the first buffer and the remaining MUXes. Finally, when C="11....11"=$2^K - 1$, the path goes through all buffers and MUXes, making it the longest path. The key is to find the C value that allows propagation of a transition from input to output of RDL in just one clock cycle in presence of noise. This C value is further analyzed for understanding the amount of noise incurred by the applied pattern.

It is noteworthy that even for the same control vector C, the total delay varies at different supply voltages. When the delay line is always reconfigured to be constant (e.g., one clock cycle), the variance of the control vector C represents the fluctuation on the power supply, assuming the temperature stays about the same. In this way, the magnitude of power supply noise can be measured and converted to a digital value. The more the noise on the RDL is, the lower the speed of the buffers and MUXes in the sensor is. Thus, the transition takes more time to go through the RDL resulting in an error, signaling that a smaller C value is needed.

2. Transition Generation (TG) Cell: TG cell is inserted at the input of the reconfigurable delay line as shown in Fig. 2, which consists of two MUXes and a launch scan flip-flop (SFF). Transitions at the input of the RDL is generated depending on the circuit operation mode:

- *Functional and Scan Modes*: In these modes, when a workload or a test pattern is applied, the sensor must be able to measure the delay of the RDL in every clock cycle based on the applied C input. Thus, clock signal "CLK", or the inverted clock "CLKB", can be fed into the reconfigurable delay line when a series of rise transitions ("Transition_type=0") or fall transitions ("Transition_type=1") are needed.
- *Launch-to-Capture Mode*: In this mode, initial values can be shifted in during scan mode ("Scan_en=1") to the launch SFF generating the desired transition at launch cycle. In this mode, only one transition is needed when "Scan_en=0" in either launch-off-capture (LOC) or launch-off-shift (LOS) scheme. Figure 2 shows the scan path (SI to SO) going through the FFs in the PSN sensor. Shifting certain values into the three scan FFs will ensure (1) generating a

rise/fall at TG cell during launch cycle in delay test and (2) 1/0 at the capture SFF and the sticky SFF as the initial value.

3. Transition Capture (TC) Cell: TC cell is implemented at the end of the reconfigurable delay line to capture transitions. It consists of two SFFs, namely capture SFF and sticky SFF, and a combinational logic to decide whether any of the transitions is not captured properly.

Let us assume the type of transition applied to RDL is rise ("Transition_type=0"). The initial values Q_1 and Q_2 at capture SFF and sticky SFF, respectively, are both set to 1 during scan mode. If a rise transition is not captured, Q_1 becomes 0, and so does Q_2 after one cycle. Then, Q_2 at the sticky SFF stays low even if later Q_1 becomes 1 again after a successful capture of rise transition. Later, when Q_2 is shifted out for analysis, we know that there has been at least one transition failed to be captured during measurement due to a large noise. C value then should be reduced further to make the path shorter; the pattern application is repeated until the path passes the test. The C value that makes the path passes the test thus represents the amount of supply voltage fluctuation on the power/ground lines. Generally, the smaller the C value is, the more noise has appeared on the power/ground lines.

Control vector (CV) unit is the second main component in the TSUNAMI architecture, as shown in Fig. 1. CV unit applies C values to the PSN sensors. Note that hereafter we use C value and control vector intermittently as both represent the select signals for the PSN sensors.

In the CV unit, control signals are applied to all PSN sensors from the scan chain, which includes K-bit control vector C and 1-bit "Transition_type". The scan chain is controlled by the external tester. The C value is shifted into the scan chain which goes to all sensors. Then the workload is applied to the chip and the PSN sensors start capturing transitions generated by the TG cell. After the workload application is over, results in terms of whether the transitions are captured at each sensor are shifted out for analysis. If a new round of measurement is needed, a new control vector (C) is generated and the same procedure is repeated. The collected data is then analyzed for each sensor to obtain the amount of noise each sensor has experienced.

3. CALIBRATION

Calibration is required before noise measurement to establish a mapping relationship between C value and supply voltage. This process begins under no or little background noise condition to identify the C value that makes the path delay one clock cycle. To achieve this, a stable V_{dd} must be applied to the sensor. To analyze the impact of noise on the sensor, new supply voltage V_{dd} is generated and adjusted at a fine granularity and applied to the entire circuit. PSN measurements are performed for each selected $V_{dd} = v_i$. The measurement results (i.e., control vectors) serve as calibration values for given V_{dd}. In other words, a mapping relationship between control vector C and supply voltage V_{dd} is established. Note that, as temperature also plays a role in circuit delay, the calibration process should be performed at similar temperature to that during noise measurement, so that the impact of temperature on delay can be canceled out. This can be achieved by warming up the circuit under test using the workload for measurement before we actually perform calibration. We also assume there are certain on-chip methods [7][8] in place to measure temperature in order to verify that temperature during calibration is indeed close to that during measurement.

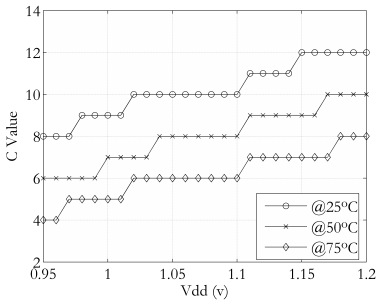

Figure 3: Relationship between V_{dd} and control vector C value (obtained using rise transitions).

An example of HSpice simulation is shown in Fig. 3. A 4-stage (K=4) RDL is implemented in a PSN sensor designed in 90nm technology. Supply voltage is adjusted at granularity of 10mV during calibration. The nominal voltage V_{dd}=1.2V. Decreasing V_{dd} represents voltage noise being generated in the circuit. As V_{dd} decreases, C value also decreases accordingly; a smaller C makes the path delay shorter. For the path to fail for the applied transition, more noise must be applied. This same calibration procedure is tested at different temperatures, i.e., 25^oC, 50^oC, and 75^oC, in this example. However, note that in practice the calibration procedure only needs to be performed once at the equivalent temperature during the measurement mode. Figure 3 clearly shows that measurement results when there is power supply noise in the background can be translated to the magnitude of PSN. Note that rise transitions are used to obtain the relationship shown in Fig. 3. The mapping relationship obtained from fall transitions is slightly different.

It is also noteworthy that measurement results for the same V_{dd} can differ across individual PSN sensors due to process variations. No process variations have been applied to the PSN sensor in this example. However, we will apply variations to the sensor and the results are shown in Section 5 for various process corners.

4. PROBLEM MODELING AND DESIGN FLOW

The design goal of TSUNAMI architecture is to provide the maximum measurement resolution on power supply noise within the budget of area overhead. In this section, we first model the problem of designing the PSN sensor and present the design flow. Then, we analyze the measurement resolution and calibration/measurement time.

1. Problem Modeling: Suppose we need to design a K-stage PSN sensor for a circuit that operates at a clock cycle of T_{clk}. We also assume that the nominal delays of the minimum-sized buffer and the MUXes are t_b and t_x, respectively. In order to ensure that the delay of the RDL meets the one-cycle requirement, the control vector value C must satisfy the equation below:

$$K * t_x + (C + m) * t_b = T - \Delta - \varepsilon * t_b, \qquad (1)$$

where Δ is a combinational effect of: (i) the delay of TG cell, (ii) the setup time of the flip-flop in the TC cell, as well as (iii) clock variations. $0 \leq \varepsilon < 1$ so that the C value just meets the requirement. m is the number of buffers in the fixed stage within the delay line.

Due to process variations, voltage noise, and temperature, the actual delay can vary in the range of $[t_{b,min}, t_{b,max}]$ and $[t_{x,min}, t_{x,max}]$, respectively. Δ can also vary in a similar way. Consequently, C will also vary from C_{min} to C_{max} as

described below.

$$K * t_{x,max} + (C_{min} + m) * t_{b,max} = T - \Delta_{max} - \varepsilon_1 * t_{b,max}, \quad (2)$$

$$K * t_{x,min} + (C_{max} + m) * t_{b,min} = T - \Delta_{min} - \varepsilon_2 * t_{b,min}, \quad (3)$$

$$0 \leq C_{min} < C_{max} \leq 2^K - 1. \quad (4)$$

where $0 \leq (\varepsilon_1, \varepsilon_2) < 1$.

Clearly, the measurement resolution is confined by the number of different observable C values $Diff = C_{max} - C_{min} + 1$, whereas the area overhead is determined by the number of stages K. Therefore, the design problem of finding the optimal K for the PSN sensor design can be expressed below:

$$\text{Maximize: } Diff = C_{max} - C_{min} + 1, \quad (5)$$

$$\text{Subject to: } 0 \leq C_{min} < C_{max} \leq 2^K - 1, \quad (6)$$

$$K \leq K_{budget}. \quad (7)$$

where (5) reflects the efforts to maximize measurement resolution; (6) shows that PSN sensor must be capable of covering the full range of timing variations due to process, supply noise, and temperature, shown also in (2)-(4); (7) is a constraint that overhead budget on stage count K should be met.

Next, we study the measurement resolution and calibration/measurement time:

• *Measurement Resolution:* Delay is determined by supply voltage V_{dd} and threshold voltage V_{th} for a circuit under given temperature. Approximately, $delay \propto \frac{V_{dd}}{V_{dd} - V_{th}}$. Without loss of generality, we assume all the devices in the circuit have a universal delay that increases from *delay* to $delay' = delay * \gamma$, when the circuit experiences a voltage drop from V_{dd} to V'_{dd}. That is,

$$\gamma = \frac{t'_x}{t_x} = \frac{t'_b}{t_b} = \frac{\Delta'}{\Delta} = n * \left(\frac{1-h}{n-h}\right), \quad (8)$$

where $n = \frac{V'_{dd}}{V_{dd}}$ and $h = \frac{V_{th}}{V_{dd}}$.

We further assume that when supply voltage drops from V_{dd} to V'_{dd}, the right C value reduces accordingly from C to C'. Based on (8) and (1), we can obtain the following

$$C - C' = \frac{\gamma - 1}{\gamma} * \frac{T_{clk}}{t_b} - (\varepsilon - \varepsilon'), \quad (9)$$

where $(\varepsilon - \varepsilon') \in (-1, 1)$.

To have two distinguishable voltage levels V_{dd} and V'_{dd}, it requires that C and C' are measured at different values (i.e., $C - C' \geq 1$). Thus, we can derive the lower bound for the measurement resolution that can distinguish V'_{dd} from V_{dd} as

$$min(n = \frac{V'_{dd}}{V_{dd}}) > \frac{1}{1 + 2 * \frac{t_b}{T_{clk}} * (\frac{1}{h} - 1)}. \quad (10)$$

The derived lower bound is in line with our intuition that for a given clock frequency faster buffers can provide better measurement resolution on the power supply noise.

• *Calibration and Measurement Time:* The calibration time T_{calib} and measurement time T_{meas} under the worst case can be obtained as:

$$T_{calib} \leq t_{calib} * (\lceil log_2(C_{max} - C_{min} + 1) \rceil + N - 1), \quad (11)$$

$$T_{meas} \leq W * t_{meas} * (\lceil log_2(C_N - C_1 + 1) \rceil). \quad (12)$$

where t_{calib} (t_{meas}) is the time it takes to shift in the control vector and to check whether it passes the calibration (measurement). N is the number of different voltage levels considered in the calibration, ranging from $V_{dd,1}$ to $V_{dd,N}$ ($V_{dd,1} < V_{dd,N}$). A binary search can be performed in the range from C_1 to C_N, which are respectively the C values found during calibration for $V_{dd,1}$ and $V_{dd,N}$. W is the number of workload under study. For example, if $C_{min} = 4$, $C_{max} = 13$, $C_1 = 6$, $C_N = 10$, and $N = 26$ different voltage levels, the total time $T_{total} = T_{calib} + T_{meas} \leq 29t_{calib} + W * 3t_{meas}$.

2. Design Flow: According to (5)−(7), we can design the PSN sensor using the flow shown in Algorithm 1. The largest stage count K that is within budget and can provide maximum difference between C_{max} and C_{min} gives the optimal design for the best measurement resolution achievable.

```
   Input:
   T_clk, Δ_max, Δ_min, t_b,max, t_b,min, t_x,max, t_x,min, K_budget
   Output:
   K_opt, m_opt
 1 begin
 2     initialize K with a relatively small value
 3     MAX_Diff = 0
 4     while K ≤ K_budget do
 5         calculate m, C_min, C_max according to (2)− (4)
 6         if C_max − C_min ≥ MAX_Diff then
 7             K = K + 1
 8         else
 9             break out of the while-loop
10         end
11     end
12     return (K_opt, m_opt) = (K, m)
13 end
```

Algorithm 1: PSN sensor design flow.

5. RESULTS AND ANALYSIS

In this section, we evaluate TSUNAMI using HSpice simulations. TSUNAMI is implemented in 90nm technology and the clock frequency for the circuit under test is 1 GHz. We intentionally selected a high frequency for the circuit to demonstrate the efficiency of TSUNAMI for measuring noise for modern designs. To evaluate the sensitivity of TSUNAMI to power supply noise and process variations, we apply various power supply noises to PSN sensors at different process corners and temperatures. Based on the simulation results, we will then estimate the measurement resolution at lower technology nodes. Note that, due to lack of space, in this paper, we only provide results for rise transition; calibration and measurement results from fall transitions are almost the same.

The variations considered in the experiments are: 10% (3 sigma) variation on the effective channel length L_{eff}, and 15% (3 sigma) variation on the threshold voltage V_{th}. As Monte Carlo simulations are extremely time consuming for HSpice, we obtained three corners, i.e., *nominal*, *slow*, and *fast*, and perform simulations on these corners. We perform calibration and measurements for sensors at the three process corners to evaluate the impact of process variations. Meanwhile, three different temperatures 25^oC, 50^oC, and 75^oC are also used in the simulations to show the impact of temperature as well.

As mentioned earlier, TSUNAMI has two operation modes: calibration and measurement. First, we apply different supply voltages V_{dd}'s to the PSN sensors (K=4) at a granularity of 10mv in the range of $[0.95v, 1.20v]$, where $1.2v$ is the nominal supply voltage and $0.95v$ represents more than 20% drop from the nominal voltage level. Note that during calibration background workload is quiet. Mapping relationship between V_{dd} and control vector is then established. The results are shown in Table 1. Each C value corresponds to a specific range of V_{dd} for the given process corner and tem-

Table 1: Mapping relationship between C value and V_{dd} (v) obtained during calibration.

Corner&Temp.		C Value											
		0-3	4	5	6	7	8	9	10	11	12	13	14-15
Slow	25^oC	<0.95				0.95-0.97	0.98-1.02	1.03-1.06	1.07-1.14	1.15-1.19	1.20	>1.20	
	50^oC	<0.95		0.95	0.96-1.03	1.04-1.08	1.09-1.15	1.16-1.20	>1.20				
	75^oC	<0.95	0.95-1.00	1.01-1.05	1.06-1.15	1.16-1.20	>1.20						
Nominal	25^oC	<0.95				0.95-0.97	0.98-1.01	1.02-1.10	1.11-1.14	1.15-1.20	>1.20		
	50^oC	<0.95		0.95-0.99	1.00-1.03	1.04-1.10	1.11-1.16	1.17-1.20	>1.20				
	75^oC	<0.95	0.95-0.96	0.97-1.01	1.02-1.10	1.11-1.17	1.18-1.20	>1.20					
Fast	25^oC	<0.95					0.95-0.97	0.98-1.05	1.06-1.09	1.10-1.16	1.17-1.20	>1.20	
	50^oC	<0.95			0.95-0.98	0.99-1.06	1.07-1.11	1.12-1.20	>1.20				
	75^oC	<0.95		0.95-0.96	0.97-1.05	1.06-1.12	1.13-1.20	>1.20					

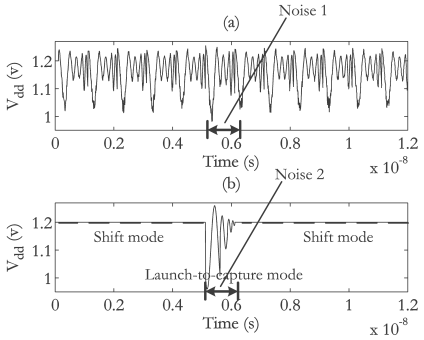

Figure 4: Power supply noise applied during measurements: (a) functional mode and (b) test mode.

perature. This clearly shows that PSN sensors are sensitive to process variations and temperature. As long as the temperature during calibration and that during measurements are similar, they should share the same mapping relationship between V_{dd} and C value.

From Table 1, we can obtain the measurement resolution on average to be about $53mv$ for the 90nm technology. It is calculated from dividing the voltage range of $[0.95v, 1.2v]$, which is $250mv$, by the average count of different C values in each case, which is 4.7. Note that for different temperature the measurement resolution can be different. For example, average measurement resolution when temperature is 75^oC is calculated to be $58mv$, while resolution when temperature is 25^oC is $50mv$. We can also verify the measurement resolution bound calculated from (10). For example, when the sensor is at the fast corner, the bound of measurement resolution is calculated to be $\frac{V'_{dd}}{V_{dd}} > \frac{1}{1+\frac{2*41}{1000}*(\frac{1}{0.4}-1)} = 89\%$. This means that for any two voltage levels, as long as they have more than 11% difference in between, their C values should be different. According to the results from Table 1, in the worst case, the indistinguishable voltage levels are $0.97v$ and $1.05v$ when temperature is 75^oC. The difference is $0.97/1.05 = 92\% > 89\%$. This verifies that the bound $\frac{V'_{dd}}{V_{dd}} > 89\%$ indeed holds.

In the next step, we apply power supply noise of different magnitudes to the circuit. Two cases of noise (Noises 1 and 2) are generated to represent functional mode and test mode noises, respectively. Segments of the noises are shown in Fig. 4. Specifically, Noise 1 has a mean value of about $1.16v$ during the period specified in Fig. 4(a), which mimics the power supply noise we have seen from silicon in functional mode; Noise 2 mimics a typical noise during test mode (launch-to-capture cycle), where the average voltage level in a clock cycle drops to about $1.15v$ (and the lowest voltage level reaches at $0.96v$). They are applied as V_{dd} to the PSN sensors. Note that without loss of generality, noises are only applied at V_{dd} while ground line does not experience noise throughout the simulation. However, noise on ground line will affect the results in a similar manner as in power line.

When power supply noise is applied, PSN sensors at different process corners and temperatures measure V_{dd} with noise and the results are shown in Table 2. C values are control vector results from the measurements, *Meas.* values are V_{dd} measured by comparing the C values in measurement and those in calibration (Table 1).

Table 2: Measurement results for noise.

Process@Temp.		Noise 1 (actual: ∼ 1.16 v)		Noise 2 (actual: ∼ 1.15 v)	
		C	Meas. (v)	C	Meas. (v)
Slow	25^oC	11	1.15-1.19	10	1.07-1.14
	50^oC	9	1.16-1.20	8	1.09-1.15
	75^oC	7	1.16-1.20	6	1.06-1.15
Nominal	25^oC	12	1.15-1.20	11	1.11-1.14
	50^oC	10	1.17-1.20	9	1.11-1.16
	75^oC	7	1.11-1.17	7	1.11-1.17
Fast	25^oC	12	1.10-1.16	12	1.10-1.16
	50^oC	10	1.12-1.20	10	1.12-1.20
	75^oC	8	1.13-1.20	8	1.13-1.20

For example, when Noise 1 is applied and the sensor at the slow corner when temperature is 25^oC reports C value at 11, we can look up this value from Table 1 and find that it represents $1.15-1.19v$ during calibration. Therefore, Noise 1 is measured to be somewhere in that range, which is consistent with the average level of $1.16v$. There are a few measurements that are slightly off, such as Noise 1's measurement at nominal corner when temperature is 50^oC ($10mv$ deviation) and Noise 2's measurement at slow corner when temperature is 25^oC ($10mv$ deviation). An important reason is that TSUNAMI captures not only a combined effect of noise and temperature, but also clock jitter and setup time variation of the flip-flop in the TC cell. These effects can result in a different mean voltage level within a measurement clock cycle even for the same supply noise. Thus, the noises seem as if they are in a slightly different range compared with other measurements. Nonetheless, they show the same combined effect of timing uncertainty that the functional circuit is experiencing.

In the above simulations for 90nm technology, the average measurement resolution is about $53mv$. For lower technology nodes, we expect the resolution to be higher based on the analysis in Section 4. Although we do not have simulation available for these technology nodes, we would like to provide an estimation on measurement resolution for 45nm and 32nm technologies.

Suppose buffer delay at 45nm and 32nm technologies is 26ps and 18ps for nominal corner at room temperature, respectively. We assume that the ratios of $\frac{t_{b,max}}{t_b}$ and $\frac{t_{b,min}}{t_b}$ at these technology nodes are equal to that at 90nm technology. Thus, we can estimate $t_{b,max}$ and $t_{b,min}$ to be the values listed in Table 3. Using these delay values in the PSN sensor design flow (Algorithm 1) we obtain K, m, C_{max}, and C_{min} for each technology node. Thus, $C_{max} - C_{min} + 1$ indicates totally how many different C values are available for distinguishing power supply noise. In addition, we assume the voltage measurement range is still $250mv$, the same as that in our simulation for 90nm technology. Hence, we can project the measurement resolution for 45nm and 32nm based on the additional different C values rendered by the faster devices, assuming the improvement on measurement

Table 3: Measurement resolution at different technology nodes when $T_{clk} = 1ns$.

Technology	MUX's Delay (ps)			Buffer's Delay (ps)			Sensor Design					resolution (mv)
	t_x	$t_{x,max}$	$t_{x,min}$	t_b	$t_{b,max}$	$t_{b,min}$	K	m	C_{max}	C_{min}	$C_{max} - C_{min} + 1$	
90nm	108	175	104	42	67	41	4	0	13	4	10	53
45nm	67	108	64	26	42	25	5	0	23	8	16	33
32nm	47	76	45	18	29	17	5	8	31	9	23	23

Table 4: Comparison with SKITTER [12]

Technology	SKITTER		TSUNAMI			
	Stage Cnt.	Trans. Cnt.	Stage Cnt.	Trans. Cnt.	$\Delta Area$	ΔT_{meas}
90nm	143	13728	4	262	51X ↓	∼ 2X ↑
45nm	231	22176	5	338	65X ↓	∼ 3X ↑
32nm	334	32064	5	370	86X ↓	∼ 4X ↑

resolution is proportional to the increase of different C values observable. It is noteworthy that the measurement resolution estimated in this way is the same as that estimated by the resolution bound from (10), which only takes into account the nominal buffer delay (t_b). This suggests that one can estimate the achievable measurement resolution quickly according to (10).

Note that in Table 3 the number of buffers in the fixed stage (m) for 90nm and 45nm designs are both 0. In other words, there is essentially no fixed stage in these two designs. However, $m = 8$ for 32nm PSN sensor design, which indicates that there should be a fixed stage consisting of 8 buffers in the RDL. The benefit of this is that without the fixed stage C_{max} will have to be increased to 39, which is beyond what a 5-stage design has to offer - the fixed stage inserted can therefore avoid an otherwise 6-stage design that incurs much larger overhead while the achievable resolution is still equivalent.

Next, we examine the area overhead of the PSN sensor and compare it with SKITTER sensor [12]. The overhead of a K-stage PSN sensor comes from: (i) $K + 3$ MUXes in the RDL and in the TG and TC cells, (ii) $2^K + m$ buffers, (iii) 3 scan flip-flops, and (iv) 2 extra logical gates (AND and OR) in TC cell. In contrast, the original SKITTER sensor requires at least $\frac{3*T_{clk}}{t_{inv}}$ stages to ensure that transition edges of 3 clock cycles can be covered, where t_{inv} is the inverter delay. Thus, it has equivalently $\frac{6*T_{clk}}{t_b}$ stages. Each stage has 1 inverter, 2 FFs, 1 AND, 1 OR, and 1 XOR. When technology scales down into 45nm and 32nm technology, each SKITTER sensor tends to have increasing number of stages, thereby larger area overhead. Thus, stage count and transistor count for TSUNAMI PSN sensor and SKITTER sensor are estimated at different technology nodes as shown in Columns 2 through 5 of Table 4. Note that for 90nm technology we calculate the stage count of SKITTER sensor to be 143, which is different from that in the original SKITTER (i.e., 129 [12]), due to probably different inverter delay and clock cycle. Nevertheless, the trend can be clearly seen that TSUNAMI sensor provides a light-weight solution for power supply noise measurement, at a 51 to 86 times smaller area overhead compared with SKITTER as shown in Column 6 ($\Delta Area$) of Table 4.

Based on (11) and (12), we can also see that TSUNAMI takes about 2 to 4 times longer measurement time than SKITTER as shown in Column 7 (ΔT_{meas}) of Table 4. This is because that TSUNAMI requires multiple runs to find out the right C value. However, it is considered worthwhile to trade some extra time spent during silicon validation for the significantly reduced area overhead on every chip. Take a 32nm one-million-transistor design for example; if we implement 50 sensors on the chip, the area overhead would be 3.2% for SKITTER whereas only a negligible 0.04% for TSUNAMI.

6. CONCLUSIONS

The proposed TSUNAMI architecture provides a low-cost and light-weight solution to measure timing uncertainty induced by voltage drop and temperature in integrated circuits. TSUNAMI can work at different operation modes, hence is helpful for speed characterization under various workloads and test conditions. Simulation results show that TSUNAMI offers high resolution at low technology nodes at significantly reduced area overhead compared to existing work.

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