Full-Circuit SPICE Simulation Based Validation of Dynamic Delay Estimation

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***Abstract*— Power supply noise may have big impacts on the design performance in the latest technologies. Accurately mapping the IR-drop effect to real delay is a challenging task, which will directly impact the accuracy of IR-drop related performance evaluation, test, and diagnosis. In this paper, we first present our previous work on setting up an IR2Delay database for addressing this issue. We then propose a flow to validate this database by comparing it with full-circuit SPICE simulation results. In this flow, mixed-signal simulation is used, which can reuse the existing digital testbench as stimuli while maintaining the accuracy of SPICE simulation.**

Keywords-SPICE; mixed-signal simulation; validation; delay estimation; IR-drop

I. INTRODUCTION

Timing analysis is a very important step for validating the design performance and its test patterns [1]. There are many signal integrity (SI) issues on design that may impact its timing performance, such as IR-drop and crosstalk effects. These SI issues are pattern-dependent parasitic effects that may significantly impact the design performance to a large extent in the latest technologies.

As VLSI technology scales down to nanometer regime, it allows packing more transistors into a chip, increasing the operating frequency of transistors, and shrinking wire distance, which may result in increased switching and power density, as well as severe crosstalk effects. Furthermore, the power supply voltage is scaled down for reducing leakage current in the latest technology, which in turn compromises the noise immunity and impacts SI of the design [2] [3] [4] [5]. In this paper, we only consider the impact of power supply noise (i.e. IR-drop effect). We will take crosstalk effect into consideration in our future work.

There are several techniques used for timing analysis and validation, like transistor level simulation with SPICE, gate level simulation with Standard Delay Format (SDF) annotation, as well as pattern-independent Static Timing Analysis (STA) technique [6] [7] [8]. The SPICE [6] is the most trustable and comprehensive analog circuit simulator in industry. It is very close to real silicon data and is often used as a "golden reference" in practice. However, the SPICE is incapable of dealing with the simulations on the entire design with millions of gates due to its computation complexity. The SDF-based gate-level simulation is much faster than SPICE simulation and is easy to be scaled up for large designs [7]. Therefore, it is widely used for logic and timing verification of the designs. The STA technique is also SDF-based, for which the timing information of each gate and interconnect is extracted from the standard library, and is annotated to the design during the performance analysis and evaluation [8]. Unfortunately, the SDF-based methods could be inaccurate because it ignores the important parasitic effects like IR-drop and crosstalk since the SDF is pattern-independent. Although there are min/typical/max delay values for best/typical/worst cases in the traditional SDF (named *static SDF*), it may still not be able to reflect the real situation accurately without considering test patterns.

The impact of power supply noise on gates and circuit performance has been addressed in several prior works. The authors in [4] proposed a layout-aware ATPG method to generate path delay test patterns for minimizing escape and perform better timing margining. In [10] and [11], the authors proposed supply voltage noise aware ATPG for minimizing the power supply noise effects on path delays to reduce yield loss. In [12], the authors presented a pattern compaction technique for IR-drop tolerant transition delay fault (TDF) pattern generation. In [13], statistical analysis is applied to evaluate the IR-drop effect on path delays. The authors in [14] proposed power noise models for array-bond and wire-bond chips for delay testing. Their models are used to compact test vectors while meeting noise and delay constraints. A look-up table is built in [15] for computing the propagation delay of the target paths under power supply noise effect. However, this model assumed linear relationship between delay and voltage, which may not be accurate. Most of the previous techniques are used for IR-drop modeling or IR-drop-aware pattern generation rather than IR-drop-aware verification or diagnosis.

In one of our previous work, we set up a database (named *IR2Delay database*) to accurately map the IR-drop of each gate in the design to its real delay variations by considering parameters such as load capacitance, transition direction, and propagation path [9]. Combined with IR-drop analysis, our IR2Delay database can update the static SDF by considering

IR-drop effect and generate pattern-dependent dynamic SDF for more accurate timing analysis.

However, none of previous work validated the accuracy of their methods by comparing with more trustable references, like silicon data or SPICE simulation results. In this paper, we propose a mixed-signal simulation based flow to validate the accuracy of our IR2Delay database by comparing with full-circuit SPICE simulation results. However, our IR2Delay database is just an example of the dynamic circuit delay estimations. It does not narrow the application scope of the proposed method, which can be applied to validate any dynamic or pattern-dependent circuit delay estimation. In the SPICE simulation, one signal is assigned to an input pin at a time, which makes it extremely difficult or even impossible for input stimuli assignment and simulation on designs with tens or hundreds of input pins. On the other hand, signal assignment of Verilog (or VHDL)–based digital simulation is very flexible and convenience. Therefore, mixed-signal simulation is used because of the following advantages:

- Reusing the existing Verilog testbench;
- Taking the advantage of the flexibility of Verilog signal assignment;
- Maintaining the accuracy of SPICE simulation.

The reminder of this paper is organized as follows. In Section II, we review our previous work on setting up IR2Delay database. In Section III, we propose the mixed-signal simulation procedure used in our validation work. Experimental results are presented in Section IV, followed by conclusions and discussions in Section V.

II. IR2Delay Database

In this section, we set up the IR2Delay database to map the average power voltage drop to the delay increase for each cell model in the library based on SPICE simulation. Mentor Graphics Eldo [16] is used for SPICE simulation, and an in-house tool was developed to automatically extract gate SPICE models from the library, set up test circuits, run simulation and extract the simulation results.

A. Transition Analysis

For each cell model in the library, we will measure its delay from all its inputs to its output for both rising and falling transitions. Clearly, when the cell has multiple input pins, there should be a transition on the on-path targeted input pin when measuring the propagation delay from it to the output of the cell. All the other input pins, which are called *off-path pins*, must have non-controlling values such that the transition on the targeted input pin can be propagated to the output. Furthermore, the status of off-path pins may impact the results. Consider a 2-input AND gate as an example. As illustrated in Figure 1, a total of seven cases should be considered when we measure the rising edge propagation delay from the input pin A to the output pin Y. The propagation delay of all these cases are measured via SPICE simulation and listed in Table I. It is easy to measure the delay in case (1) when off-path pin B is stable. If off-path pin B has a rising transition and its transition arrives earlier than the transition on pin A, as shown in case (2), pin B is stable when the transition on pin A arrived, which is the same as case (1). Similarly, for case (3), the output transition is determined by the transition on pin B, and pin A should be considered as off-path pin. For instance, due to a 2ns difference between the A and B transitions, we obtain a 2.130ns delay from pin A to pin Y.

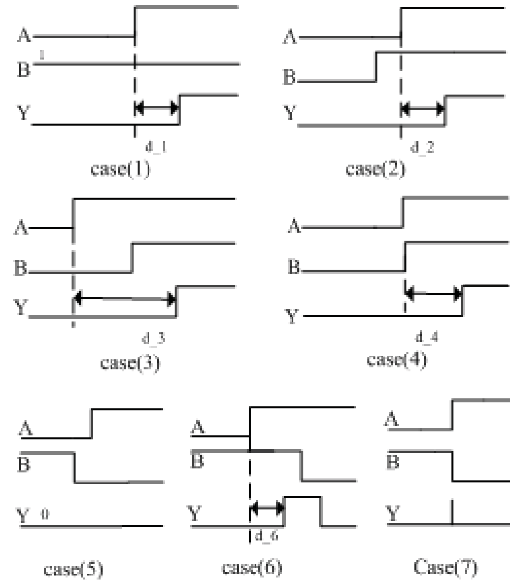

Figure 1. Rising edge transition propagation of an AND2X1 gate.

TABLE I. PROPAGATION DELAY FROM A TO Y FOR AN AND2X1 GATE (LOAD CAPACITANCE: 50FF)

Test case	Case (1)	Case (2)	Case (3)	Case (4)	Case (5)	Case (6)	Case (7)
delay (ns)	0.129	0.129	2.13	0.137	—	0.129	—

When pin B has a rising transition simultaneously with pin A, as shown in case (4), it impacts the propagation delay on pin A. From Table I we can see that the delay increase is about 6.2% compared with case (1) or (2). When pin B has a falling transition, case (5) or (7) should not be considered since they cannot ensure the transition on pin A can be propagated to the output pin Y. In other words, the falling transition on pin B has to arrive later than pin A's transition, as shown in case (6). In this case, the rising transition propagation delay from A to Y is also the same as what we experience in case (1). In summary, the rising edge propagation delay from pin A to pin Y can be measured by setting pin B to 1 as shown in case (1). Although the simultaneous transitions (e.g. case (4)) will impact the propagation delay, we can ignore it since the delay variation is small (6.2% in our experiments). The same can be applied to the falling transition propagation delay. In this paper, all

off-path pins are set to non-controlling values when measuring the propagation delay from one input pin to the output.

B. Driving Strength Analysis

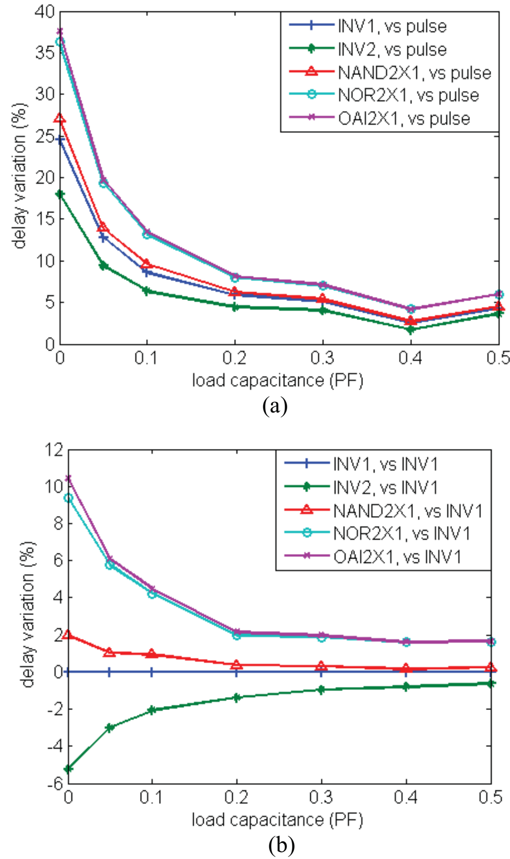

Figure 2. Delay variations of BUFX3 gate when driven by (a) different logic gates vs. pulse source driver and (b) different logic gates vs. INVX1 gate

In any design, a non-primary input (PI) gate is driven by another gate with finite driving strength. A non-PI gate is a gate that none of its inputs is directly connected to a PI. The driving strength of the driving gate can also impact the propagation delay on the targeted driven gate. Consider a buffer cell (BUFX3) as an example. Figure 2 shows the delay variations between the driving gates vs. pulse source (a) and the delay variations between the driving gates vs. INV1 gate (b), with different output load capacitance of the targeted driven gate. The pulse source in this paper refers to the ideal pulse signal with infinite driving strength in SPICE simulator.

From the above figures, we can see that with the increase in load capacitance, the delay variations of different driving gates are reduced. Regardless of the output load capacitance, the delay variation between gate driver and pulse source driver is significantly larger than the delay variation between various gate drivers and INV1 gate driver. Therefore it is more accurate to drive the targeted driven gate with a logic gate, rather than with a pulse source, when measuring its gate delay. These delays may vary for different driving gates, but the variation is small and hence can be ignored to simplify and speed up the procedure. In our experiments, we select an appropriate driving gate to drive the targeted gates when measuring their delays. The appropriate driving gate is a gate with sufficient driving strength to drive the test gate.

C. Power Voltage-Delay Map

An in-house tool was developed to perform SPICE simulation and set up the IR2Delay database. For each cell model in the library, we run SPICE simulations and measure its propagation delays with

- different propagation paths, from all input pins to the output pin;
- different transition directions, including rising and falling transitions;
- different power voltages;
- different load capacitances.

As mentioned in subsection II-A, when measuring the propagation delay from one input pin to the output pin, the off-path pins are kept to be stable non-controlling values. The logic gate with proper driving strength is selected to drive the targeted gate as discussed in subsection II-B.

The simulation results are written into an IR2Delay database. Generally speaking, a large IR-drop will result in a large delay increase. However, for different gates, the same IR-drop will result in different extra delays. The relationship between IR-drop and delay increase of all cells are reflected in the IR2Delay database.

The size of IR2Delay database depends on the number of cells in the library, number of input pins of each cell, as well as the number of discrete power voltages and output load capacitance defined by the user. In our experiments, we use 180nm Cadence Generic Standard Cell Library, with a combination of 40 different power voltages and 8 different output load capacitance, and size of our IR2Delay database is approximate 700KB.

III. MIXED-SIGNAL SIMULATION-BASED VALIDATION

From the discussions in Section II, it can be seen that several approximations are introduced when setting up IR2Delay database to make the procedure feasible to be applied to industrial designs, like:

- Using lumped output load capacitance instead of distributed RC network in real case;
- Using a fixed driving gate to drive the target gate under test instead of various driving gates with different driving strength in the design;

- Using average IR-drop values instead of dynamic IR drop instantaneous values in real situation.

Therefore, the accuracy of the IR2Delay database has to be validated before being applied to real applications. This work will focus on validating our IR2Delay database.

The best way to validate the IR2Delay database is to compare with the real silicon delays, which are very difficult to measure. However, we can validate our procedure by comparing with SPICE simulation, which has been proven to be very close to real silicon and is often used as a “golden reference” in industry.

A. Mixed-Signal Simulation

The IR2Delay database can perform accurate delay calculation for a given pattern set. In order to validate the IR2Delay database calculation results, we have to apply the same patterns to the design and run full-circuit SPICE simulation. A design may have a large number of input/output pins. In SPICE simulation, the input signal waveform has to be specified one at a time, and thus it is very difficult to translate the existing patterns to analog stimuli signals for SPICE simulation. Figure 3 shows a sample waveform and its description in the SPICE netlist. If the signal waveform is not a regular pulse with a fixed frequency like the clock signal, it has to be in a piecewise format as shown in Figure 3, in which every transition point of the signal has to be specified. It is very tough and time-consuming considering that a signal may have multiple transitions and a design may have multiple input pins need to be specified. Furthermore, to the best of our knowledge, there is no available tool can be used to transition digital test pattern to analog stimuli in SPICE format. Therefore, a mixed-signal simulation method is proposed for the SPICE design activation and simulation, as shown in Figure 4.

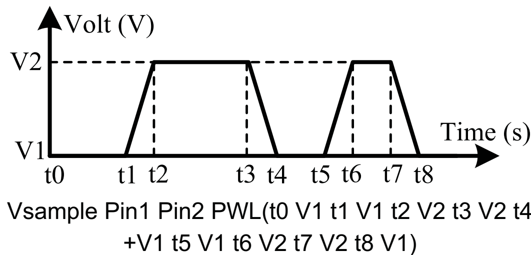

Figure 3. A sample waveform and its description in the SPICE netlist.

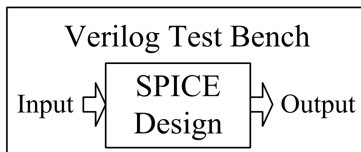

Figure 4. The structure of mixed-signal simulation.

As shown in Figure 4, the Verilog testbench, which was dumped from ATPG tool, is used to stimulate the SPICE design under test. Hence, we can reuse the ATPG testbench and take both advantages of the flexibility of Verilog assignment and the accuracy of SPICE simulation. Mentor Graphics ADMS [17] was used for the mixed-signal simulation. Virtual D/A and A/D converters are needed between the Verilog testbench and SPICE design. The D/A converter is used to translate the digital stimuli from the Verilog testbench to analog signals so that they can be applied to the SPICE design. The A/D converter is used to translate the output signals of the SPICE design to digital data, so that the Verilog testbench can read it.

Figure 5 shows an example of command lines for running Mentor Graphics ADMS. Line 1 and line 3 are used to create the digital library and ADMS library, respectively. Line 2 is used to compile the *s344* module file *s344_define.v*, which includes the s344 pin definition in Verilog format. The pin definition in the SPICE netlist is consistent with it. Line 4 is used to compile the s344 sub-circuit into the s344 module. It will connect the SPICE sub-circuit to the corresponding pins of the digital module compiled in Line 2. Line 5 is used to compile the test pattern file in Verilog format to obtain the testbench module *s344_pat_v_ctl*, which is used in Line 6. The ADMS simulator is invoked in Line 6. The command file *mycmd.cmd* includes necessary SPICE libraries, SPICE *.MEASURE* commands for delay and average power voltage measurement, definitions of D/A and A/D converters, power definition and any user-defined options for SPICE simulation. Line 7 is used to run the simulation.

```
1: valib diglib
2: vlog s344_define.v
3: valib admslib
4: vaspi -f -srclib diglib -work admslib s344_module
s344_subckt@s344 _top.sp
5: valog s344_pat_1.v
6: vasim -c s344_pat_v_ctl -cmd mycmd.cmd
7: run -all
```

Figure 5. A sample command lines for running Mentor Graphics ADMS.

B. Simulation Results Extraction

It is very time-consuming, and sometimes impossible for large designs, to measure the delay of each gate in the waveform database resulting from SPICE simulation. Therefore, we develop two procedures to automate this validation work, as shown in Figure 6.

Procedure 1: This procedure is used to pre-process the SPICE netlist of the design. It will parse the SPICE netlist for information of all the gates and their corresponding pins (input, output, and power pins). Thus it can enable the simulator to measure the delay and average power supply voltage of each gate in a specific timing window using the SPICE *.MEASURE* command. The timing window is between the launch and capture clock cycles of our test pattern.

Procedure 2: This procedure is used to post-process the simulation results. In Procedure 1, the delay and average power supply voltage of all the gates in the design are measured. However, for a specific test pattern, not all the gates can be sensitized. This procedure will identify the gates sensitized between the launch and capture clock cycles and extract their valid delay and average power supply voltage. For the sensitized gates with multiple inputs, if more than one input has transitions, the procedure will determine which input transition is the valid one and extract the delay from the valid input pin to the output pin. The measured average power supply voltage is used to search the IR2Delay database for the validation.

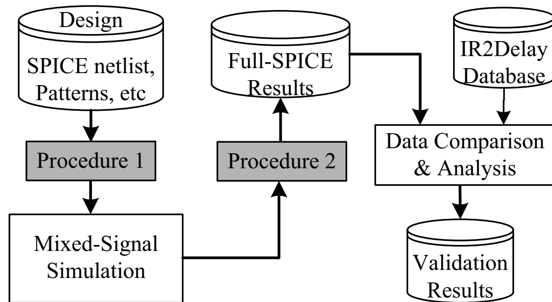

Figure 6. The flow of our mixed-signal simulation-based validation procedure.

After simulation results are extracted, we search the IR2Delay database for gate delays according to the power supply voltage, propagation path, transition direction, and output load capacitance of the sensitized gates. Therefore, we can compare the IR2Delay database results with full-circuit SPICE simulation results to see whether our IR2Delay database is accurate enough for mapping the IR-drop to real gate delays.

IV. Experimental Results

Since the full-circuit SPICE simulation is very time-consuming for large circuit, we use a small benchmark circuit from ISCAS, s344, for our validation purpose. 180nm Cadence Generic Standard Cell Library with typical 1.8V power supply voltage was used in our experiments. Synopsys Design Compiler [8] was used for logic synthesis, and Astro was used for physical design. Mentor Graphics FastScan [18] was used for pattern generation. Mentor Graphics Eldo [16] and ADMS were used for SPICE simulation and mixed-signal simulation. The IR2Delay database procedure was implemented with Perl, and pre-process and post-process procedures for mixed-signal simulation were implemented in C/C++.

We chose a test pattern from transition delay fault test pattern set generated for s344, for which there are 32 gates being sensitized. We run full-circuit SPICE simulation on the design and extract the delays of these sensitized gates. Then we search the IR2Delay database for these sensitized gates' delays. The delay comparison between these two results is shown in Figure 7. The X axis represents the sensitized gate ID, and the Y axis represents the absolute delays of all these sensitized gates. From the figure, it can be seen that our IR2Delay database calculated delays are smaller than the delays obtained from full-circuit SPICE simulation. There are many reasons for this difference, including the approximations we made in the IR2Delay calculation, as well as ignoring the impact of some other important design parameters, like crosstalk effects, which may impact the capacitance of wires connected to the target gate, and further impact the gate delay. We will take crosstalk effects into consideration in our future work, so that we can make our calculation more accurate.

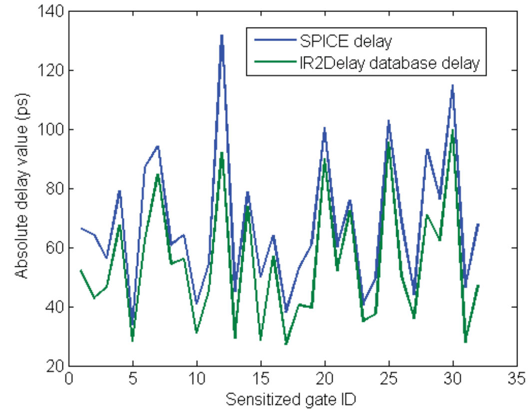

Figure 7. Delay comparison between SPICE simulation and IR2Delay database results.

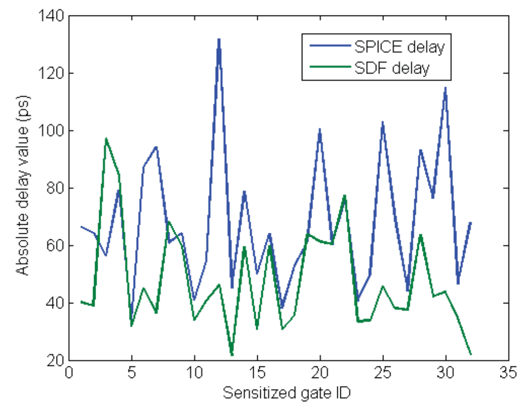

Figure 8. Delay comparison between SPICE simulation and SDF file.

Figure 8 presents the delay comparison between full-circuit SPICE simulation and SDF delays on the sensitized gates in the design. The SDF delays were extracted using commercial EDA tools. From Figure 7 and 8, it is obvious that even though the absolute values are different, our IR2Delay database correlates very well with the full-circuit SPICE simulation results comparing with the SDF delays. Table II presents the correlation coefficients of these two data pairs.

TABLE II. DELAY CORRELATION COEFFICIENTS OF DIFFERENT DATA PAIRS

Data pair	IR2Delay vs. SPICE	SDF vs. SPICE
Corr. Coeff.	0.947	0.278

The correlation coefficient is calculated with Equation (1).

$$\rho_{X,Y} = \frac{E((X-\mu_X)(Y-\mu_Y))}{\sigma_X \sigma_Y} \quad (1)$$

Where $\rho_{X,Y}$ is the calculated correlation coefficient, X and Y are the two random variables used for correlation calculation, respectively. μ_X and σ_X, μ_Y and σ_Y are expected value and standard deviation of X and Y, respectively.

From the experimental results, it is clearly that our IR2Delay database can provide more accurate delay calculation compared with SDF database. Therefore, it can be used for more accurate dynamic delay estimation.

The CPU runtime for setting up the IR2Delay database is approximately *6 hours* since tens of thousands of SPICE simulation are needed to obtain the delays of each gate under different circumstances and set up the database. However, once the database is being setup, it can be used to any designs using the target library. The computation complexity of searching the IR2Delay database is O(*log n*), where *n* is the number of logic cells in the technology library. Therefore, it is very fast and easy to scale to larger industry design.

V. CONCLUSIONS

In this paper, we reviewed our previous work of building the IR2Delay database based on SPICE simulation, to map the IR-drop of each gate in the design to real delay increase, considering average IR-drop on the gate, signal propagation path, transition direction, as well as output load capacitance. The database was validated by comparing with full-circuit SPICE simulation results. Mixed-signal simulation was proposed to take both advantages of the flexibility of Verilog signal assignment and the accuracy of SPICE simulation, and to make the procedure automatic and easy to use. Experimental results demonstrate that our IR2Delay database is more accurate than the current SDF-based delay calculation. Furthermore, it is very fast to calculate gate delays using IR2Delay database, which makes it easy to scale for larger industry design. With the IR2Delay database, we can generate pattern-dependent dynamic SDF with IR-drop consideration for accurate performance evaluation, IR-drop related failure analysis and diagnosis.

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