Analysis of Power Consumption and Transition Fault Coverage for LOS and LOC Testing Schemes

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Abstract* — **At-speed scan testing has become mandatory due to the extreme CMOS technology scaling. The two main at-speed scan testing schemes are namely Launch-Off-Shift (LOS) and Launch-Off-Capture (LOC). As it can be easily implemented, LOC has been widely investigated in the literature in the last few years, especially regarding test power consumption. Conversely, LOS has received much less attention. In this paper, we propose a comparison between the two testing schemes in terms of transition fault coverage and power consumption, in order to quantify the pros and cons of LOS with respect to LOC. This study shows that LOS not only exhibits higher performance in coverage but also does not require as much extra power as predicted, especially in terms of peak power. These facts may represent convincing arguments for its wider use and development.**

1. INTRODUCTION

Nowadays electronics products present various issues that become more important with CMOS technology scaling. High operation speed, and so high frequency, is a mandatory request. On the other hand, power consumption is one of the most significant constraints due to large diffusion of portable equipments. These needs influence not only the design of devices, but also the choice of appropriate test schemes that have to deal between production yield, test quality and test cost.

Testing for performance, required to catch timing or delay faults, is therefore mandatory and is often done through at-speed scan testing for logic circuits. At-speed scan testing consists of using a rated system (nominal) clock period between launch and capture for each delay test pattern, while a longer clock period is normally used for scan shifting (load and unload cycles).

In order to test for delay (or transition) faults, two different schemes are used in practice during at-speed scan testing: Launch-off-Shift (LOS) and Launch-off-Capture (LOC) [1, 2]. Although LOS is known to achieve higher transition fault coverage than LOC (with significantly fewer test patterns), both schemes are useful to obtain a high test quality, mainly because some faults covered by LOS are not covered by LOC and vice-versa [3]. However, LOS suffered until recently from the fact that the high-speed scan enable control signal was expensive to implement and not supported in most scan-based designs. Solutions to this problem have been proposed in [3, 4] and both schemes are now used in practice in industry [5].

Although at-speed scan testing is mandatory for high-quality transition test, its applicability is being severely challenged by test-induced yield loss, which occurs when functionally good chips fail only during at-speed scan testing [6, 7]. Both schemes (LOS and LOC) may suffer from erroneous results during test, and the major cause for this problem is Power Supply Noise (PSN), i.e., IR-drop and Ldi/dt events, caused by excessive switching activity during launch and capture cycles [8]. In order to deal with such problem, special techniques (modification of patterns, use of power management infrastructure, power-aware design-for-testability (DfT) solutions, etc.) are required during at-speed scan testing to reduce the yield loss risk induced by excessive power supply noise [9].

The LOC testing scheme has been widely investigated in the literature regarding power consumption. Numerous power-aware solutions have been proposed, ranging from automatic test pattern generation (ATPG)-based and X-filling techniques to DfT and clock stretching solutions [10, 11].

Conversely, the LOS testing scheme has been less investigated, mainly for the following two reasons: i) its use in industry that came few years after LOC, and ii) the belief that LOS consumes much more power than LOC and hence is more vulnerable to PSN. About this last point, a recent industrial analysis has been presented in [5] and shows that power consumption during launch and capture cycles for LOS may not be as high as predicted.

So, the overall objective of this study is to investigate in more details the LOS testing scheme. For this purpose, this paper presents a comprehensive and comparative analysis of LOS and LOC in terms of power consumption and transition fault coverage, so as to quantify the pros and cons of LOS with respect to LOC. The next step of this study will be to propose solutions for reducing power consumption during LOS through the use of dedicated techniques and algorithms.

This paper is organized as follows. In the next section, we give basics on LOS and LOC schemes. In Section 3, we describe the automated experimental flow for transition fault coverage measurement and power estimation. Section 4 presents complete results on transition fault coverage achieved with both schemes. In Section 5, the power analysis is described and experimental results are presented.

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Section 6 summarizes the contribution and presents a discussion on challenges of LOS.

2. BASICS ON LOS AND LOC SCHEMES

The typical waveforms of the clock and Scan Enable (SE) signals for LOS and LOC tests are given in Figure 1.

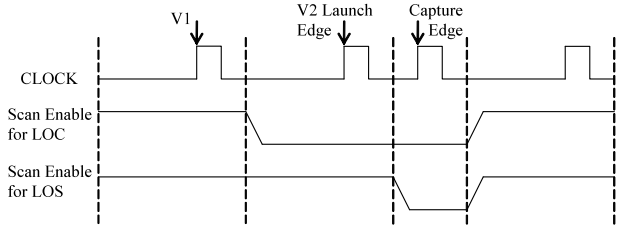

Figure 1: Waveforms of LOC and LOS

Both schemes use a two-pattern test <V1, V2> to detect a targeted transition fault. In both schemes, test vector V1 is shifted into the scan chain(s) at slow speed, while the launch-to-capture cycle (also called "test" cycle and defined as the time interval between the launch edge and the capture edge) is applied at rated speed. In LOS, the SE signal remains at '1' (shift mode) and test vector V2 is obtained by one bit shifting of vector V1. Transitions are launched and propagated in the CUT. Right before the capture cycle, the SE signal is switched from 1 to 0 (functional mode), and then the response to V2 is captured in the scan flip-flops. In LOC, after test vector V1 has been shifted into the scan chain(s), the SE signal has a large time window to be switched from '1' to '0'. This time, vector V2 is obtained by the response of the CUT to vector V1. Transitions are launched and propagated in the CUT, and the response to V2 is captured in scan flip-flops during the capture cycle [3].

The main features of LOS and LOC have already been discussed in the literature [12]. Basically, the complexity of the test generation process is lower with LOS. On the other hand, LOS is suspected to cause over-testing, *i.e.* rejecting good devices by falsely testing faults that could not be sensitized in functional mode. Nevertheless, it is reported in [13, 14] that this situation may also occur with LOC, especially when more than one clock cycle are used before final response capture. An illustration of such a scheme is shown in Figure 2.

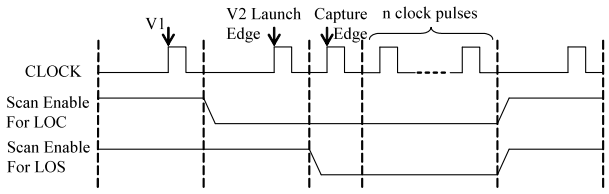

Figure 2: Using multiple capture cycles

This extension of LOC has been shown to provide higher delay fault coverage with a minimum test time penalty [14]. This extension is also applicable when LOS is used. Moreover, it is possible to combine LOS and LOC for the same purpose: fault coverage improvement. At the end, this has led to the existence of hybrids of LOS and LOC, such as LOSC (launch-on-shift-capture), LOCS (launch-on-capture-shift), or more simply LOS+LOC (successive application of LOS and LOC patterns). A LOSC (resp. LOCS) test is a three-pattern test for transition faults that launches transitions by both launch-on-shift and launch-on-capture mechanisms. More details on LOSC and LOCS can be found in [12]. We shall come back on these hybrid schemes in Section 4.

3. EXPERIMENTAL FLOW

In order to measure transition fault coverage and estimate power consumption for LOS and LOC testing schemes, we have implemented the automated flow depicted in Figure 3 and performed experiments on full scan version of ISCAS'89 and ITC'99 benchmark circuits.

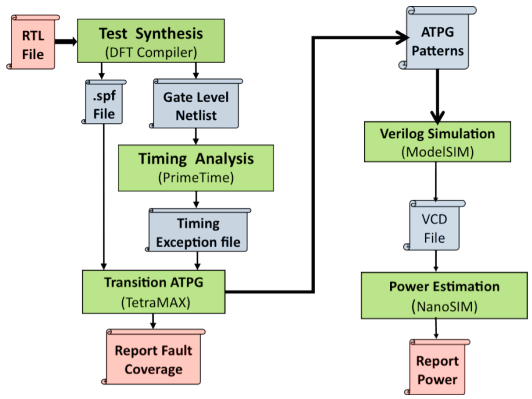

Figure 3: Automated estimation flow

The characteristics of these circuits are reported in Table 1. A single scan chain has been considered for each circuit (except for four circuits as shown in Table 1), which is a valid assumption for the purpose of comparing LOS and LOC schemes.

TABLE 1: CIRCUIT CHARACTERISTICS

Circuit	#gates	#FFs	#faults	#chains
s9234	1887	211	7114	1
s13207	3793	638	12970	1
s15850	4005	534	15026	30
s35932	10926	1728	36444	1
s38417	12361	1636	43002	1
s38584	13398	1426	52528	1
b12	1218	121	4740	1
b14	5907	245	18616	1
b15	8204	449	35040	1
b20	9825	490	38778	1
b21	10504	490	40914	10
b22	15201	735	58518	50
b17	28418	1415	108124	50

First, we use DFT Compiler® from Synopsys [15] for the scan chain insertion and test synthesis of each circuit. Next, we determine the maximum path delay in each circuit and define the nominal clock period through PrimeTime®

[16]. Transition fault test sets are then generated using TetraMAX® [17] for both LOS and LOC testing schemes. Note that we used the default setting and random filling options during ATPG for all circuits. No compaction has been used during test set generation. The primary inputs and primary outputs were not included in the scan chain, but were assumed to be held constant during scan-in and scan-out operations (low cost tester requirement). After that, fault simulation is done with TetraMAX® and provides the fault coverage measure. The test patterns are simulated using ModelSim™ [18] and the switching information for the patterns is stored in a VCD file. Then, the VCD file is used with NanoSim™ [19] to perform the power and transient analysis. The power simulations made with NanoSim™ are actual transient simulations that take in account large and small resistors and coupling capacitors [22]. Other details on power metrics will be given in Section 5.

4. FAULT COVERAGE ANALYSIS

Concerning fault coverage, a first set of experiments was done with the aim of achieving the maximum Transition Fault Coverage (TFC, expressed in %) before a given abort time limit fixed by the ATPG tool is reached. Results are reported in Table 2 for largest benchmark circuits, and are provided for both LOC and LOS schemes.

TABLE 2: TRANSITION FAULT COVERAGE EVALUATION

Circuit	LOC		LOS		LOC + LOS		
	TFC	#patt	TFC	#patt	TFC	S+	C+
s9234	77.3	597	96.4	592	99.6	1438	25
s13207	75.9	424	83.7	451	90.3	1452	314
s15850	65.6	469	95.1	817	99.9	4108	20
s35932	81.1	72	96.9	98	100	5930	42
s38417	93.7	1440	97.7	1521	99.4	1633	291
s38584	83.6	1669	97.6	1291	99.7	7535	51
b12	84.1	473	90.0	325	98.8	624	342
b14	77.7	605	97.1	1036	99.7	3939	223
b15	84.9	1551	96.5	1430	98.8	4538	461
b20	86.9	1771	96.1	1703	98.6	3937	395
b21	87.3	1993	96.2	1795	98.9	4159	520
b22	86.3	2736	86.7	2546	96.7	4632	4530
b17	87.6	3957	96.1	3455	98.1	10890	1701

A first analysis of the results shows that for most circuits, the TFC is far from being close to 100%. A more general comment is that the TFC achieved with LOS is higher than that achieved with LOC. This predominance does not change when the size of the circuit increases, or when the type of circuit changes - there is no difference between ITC'99 and ISCAS'89 circuits. It can also be noted that for small circuits, the test length (i.e. pattern count) for LOS is longer than for LOC. However, the test length for LOS becomes shorter than for LOC when the size of the circuit increases.

Although LOS test achieves higher TFC than LOC test, we can also observe that LOS generally does not achieve 100% TFC. As reported in [12], LOS-untestable faults may be tested by LOC while LOC-untestable faults may be tested by LOS. This suggests that even though LOS performs better, the combined use of LOS and LOC test is needed to achieve the highest fault coverage. In order to verify this assertion, we have evaluated the TFC when both types of patterns are used. Results are summarized in Table 2. For this purpose, we have successively applied the two sets of test patterns to each circuit, without using fault dropping during test generation. So, the test length of LOC+LOS is simply the sum of the test length of LOC and the test length of LOS (for each experimented circuit). We have arbitrarily applied LOS patterns after LOC patterns (TFC does not change if we apply LOS patterns first). We have also calculated the number of faults only covered by LOS (column S+) and those only covered by LOC (column C+). As can be seen in Table 2, the TFC achieved with LOC+LOS is confirmed to be much higher than the TFC obtained with either LOC or LOS alone. Therefore, these results demonstrate the usefulness of both types of test. Note that a similar conclusion was drawn in [3], except that results were presented only for small and middle size ISCAS'89 benchmark circuits. Here, results are extended to largest ISCAS'89 circuits and to the set of ITC'99 circuits. Further results on hybrids of LOS and LOC are presented in [12] and also show the need to combine LOS and LOC tests. It is reported that LOSC and LOS+LOC perform better than other schemes, and that both achieve comparable transition fault coverage (with a slightly higher number of patterns for LOS+LOC).

5. POWER ANALYSIS

5.1Power metrics

Power consumption has been evaluated during the launch and capture cycles of LOC and LOS testing schemes. Launch power is the power consumed during the launch-to-capture cycle, also called "test" cycle, which is an at-speed clock cycle. Capture power is the power consumed right after the capture edge, during a time interval also equal to the rated clock period of each experimented circuit. Figure 4 shows the time windows in which these power measures are made.

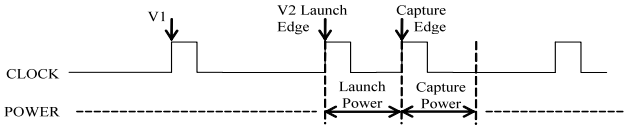

Figure 4: Launch and capture power time windows

It is reported in [20] that both launch and capture power consumption must be reduced. Excessive power consumption between launch and capture (launch power) may lead to excessive PSN that can increase gate delays, and hence path delays, in the CUT. With an increased delay, some tested paths may be slower than in functional mode of operation though being defect-free. This may lead to declaring a good chip as faulty, thus leading to manufacturing yield loss [10].

Excessive power consumption during the next clock cycle (capture power) needs to be considered as well,

especially because additional functional (at-speed) capture cycles are often used after the first capture cycle to increase fault coverage of LOC and LOS as already discussed in Section 2. Using additional functional capture cycles allows maintaining the CUT in a functional state, which not only avoids detection of certain faults that could not be sensitized in functional mode, but also avoids abnormal (excessive) switching activity during capture cycles. Note that in this case, the test response to a given pattern corresponds to the last state stored in flip-flops of the scan chain, and must not be corrupted by excessive PSN during the launch cycle and its successive at-speed capture cycles.

In fact, excessive PSN during capture may only occur during the first capture cycle (in the case where more than one capture cycle is used). This assertion has been experimentally validated in [21] on industrial circuits tested with LOC patterns. It is shown that the WSA (Weighted Switching Activity) during the functional capture cycles reaches a steady state value which is much lower than the WSA during the launch and first capture cycles, irrespective of the test pattern loaded in the scan chain(s) and the filling option (random, preferred fill or zero fill) used to replace don't care bits in the pattern. It is predicted that the same conclusion can be drawn when LOS patterns are used since this decrease of switching activity after the first capture cycle comes from the fact that the CUT operates in functional (and hence power-safe) mode. For this reason, capture power has been evaluated only during the first capture cycle in our experiments.

The power analysis has been done considering two power metrics: cycle average power and peak power consumption. Cycle average power refers to the average of instantaneous power consumed in the CUT during a single clock cycle: the launch or the capture cycle in our experiments. The time window considered for cycle average power measurement was fixed by the nominal (rated) clock period of each circuit. Peak power refers to the highest power value measured during the same single clock cycle. Both values can be evaluated for a given test pattern, generally the most power-consuming pattern, or for a complete test sequence.

5.2 Experimental Results

Experiments have been done on benchmark circuits synthesized with an industrial 90nm technology, considering a power supply voltage of 1.2V. Only dynamic switching power due to switching capacitances has been considered (short-circuit power and leakage power consumptions were neglected). This is a valid assumption for the considered technology with the purpose of comparison between LOS and LOC. In next studies, we will employ more scaled technology (<90nm), where the leakage component of the power is more important (>10%). In this case, although the impact of the leakage power component on the overall power will be more important than in present case, we expect that it will not have a sensible impact on the comparative results between LOC and LOS schemes presented in this work. This forecast is based on the fact that we expect that the major leakage power will impact the two test schemes in the same manner (the circuits and the number of scan FFs are the same, leading to similar leakage currents).

Power consumption measured with NanoSim™ during the launch cycle is reported in Table 3 for largest circuits. Results are reported in milliWatt. For both LOS and LOC, the cycle average and peak power values are reported. The peak power is the value measured for the most power-consuming pattern obtained for each circuit. The value reported for each circuit in the "C. Ave." columns is an average over the complete test sequence of the cycle average power measured for each test pattern. Similarly, power consumption measured during the capture cycle obtained for each circuit is reported in Table 4, still considering cycle average and peak power consumption. Note that all power measurements include both logic power (power in the combinational logic) and sequential power (power in scan flip-flops). Clock power (power in the clock tree) is not included.

TABLE 3: POWER ESTIMATION DURING THE LAUNCH CYCLE

Circuit	LOC		LOS	
	C. Ave.	Peak	C. Ave.	Peak
s9234	5.76	48.67	9.92	59.16
s13207	3.73	143.96	5.84	176.28
s15850	3.53	128.71	6.22	159.30
s35932	17.68	378.60	24.11	452.17
s38417	11.38	371.02	21.88	456.06
s38584	8.75	326.12	16.69	439.39
b12	0.93	26.04	1.99	40.61
b14	3.00	59.88	5.10	77.70
b15	3.20	98.15	8.80	127.08
b20	7.64	114.24	14.71	143.88
b21	8.06	116.38	15.71	144.94
b22	11.79	170.94	23.02	208.49
b17	10.93	306.29	24.85	400.63

TABLE 4: POWER ESTIMATION DURING THE CAPTURE CYCLE

Circuit	LOC		LOS	
	C. Ave.	Peak	C. Ave.	Peak
s9234	6.27	47.52	7.09	51.92
s13207	3.95	139.80	4.42	144.28
s15850	3.64	122.56	4.44	129.34
s35932	20.01	376.08	21.94	384.12
s38417	12.17	366.00	20.04	392.16
s38584	9.70	322.92	11.95	327.85
b12	1.07	25.99	1.13	26.40
b14	1.87	53.03	2.02	55.27
b15	3.66	97.08	4.26	99.00
b20	7.98	110.22	7.99	109.85
b21	7.86	116.20	8.43	112.48
b22	11.51	173.24	13.19	165.73
b17	16.48	341.93	13.13	307.30

From these results, we can make the following detailed observations:

Launch power

Although in the same level of magnitude, LOS launch

power is higher than LOC launch power when cycle average power is considered. This result was quite predictable and is in line with results already presented in [5]. On the other hand, the measures of peak power are much closer, with an average increase of about +28% and the maximal increase lower than +56% (for circuit b12). This is an important result since peak power is a more relevant parameter than cycle average power when considering PSN induced problems. The main reason is that the cycle average power may consider time windows within the clock cycle where there is no activity (especially at the end of the cycle) and hence can overestimate the level of PSN. On the other hand, peak power is more representative of the amount by which PSN, especially voltage drop, may affect the timing behavior of a CUT.

There is a noticeable difference between the results of cycle average power achieved with ISCAS'89 circuits and those achieved with ITC'99 circuits (ISCAS'89: +71% for LOS, ITC'99: +110% for LOS). Conversely, we observe a small difference between the results of peak power consumption achieved with both benchmark families (ISCAS'89: +24% for LOS, ITC'99: +31% for LOS).

Capture power

LOS capture power and LOC capture power are almost the same for cycle average power (+14% on average for LOS) as well as for peak power (+1.4% on average for LOS) measurements. From a general standpoint, this result demonstrates a similar behavior of LOS and LOC during the capture cycle.

For some benchmark circuits, LOC is even more consuming than LOS for cycle average power and/or peak power. For example, this is the case for circuit b17, one of the largest circuits of the ITC'99 family.

Launch and Capture power

LOS capture power and LOC launch power are also very similar (for both cycle average and peak power). This similarity was already observed in [5] and is attributed to the fact that LOS capture power and LOC launch power both correspond to the first functional cycle loaded into scan flip-flops.

In order to analyze the distribution of power between the combinational logic and the scan flip-flops, we performed another set of experiments. Due to space limitation, the results achieved are not detailed in this paper, nevertheless they are summarized below:

- LOS launch power is higher than LOC launch power for both combinational (+101% on average) and sequential (+87% on average) parts. This difference can be explained by a higher activity induced by LOS patterns and by the contribution of the scan enable signal that switches during the launch cycle only in the LOS testing scheme, as detailed subsequently.
- During the capture cycle, LOS sequential power and LOC sequential power are comparable, simply because LOS and LOC patterns have the same contribution and there is no difference regarding the switching of the scan enable signal between the two schemes.
- There is a significant difference concerning capture power between the ISCAS'89 and the ITC'99 families, especially regarding the combinational part. For ISCAS'89 circuits, the average increase from LOS to LOC are respectively +78% (combinational) and +14% (sequential). For ITC'99 circuits, the average variations between LOS and LOC are respectively -10% (combinational) and +8% (sequential). This shows that for ITC'99 benchmark circuits, LOS and LOC are quite similar regarding both combinational and sequential power consumption.

The previous observations were made considering the cycle average power. The values of peak power are similar for LOS and LOC when considering both combinational power and sequential power. Hence, they are not detailed and discussed in this paper.

For a more detailed power analysis of LOS and LOC, we now report the results of a transient analysis done on circuit b05 of the ITC'99 family. We show the two typical waveforms of the overall current supplied during the launch and capture cycles of LOS and LOC (respectively in Figure 5 and 6), for circuit b05 with a sampling resolution of 10ps. The transient analysis of the capture cycle does not show meaningful differences for the two testing schemes, thus it is here less detailed.

The LOS scheme exhibits three peaks during the launch cycle (peaks 1a, 2a and 3a in Figure 5), while LOC only exhibits two peaks (peaks 1b and 2b in Figure 6).

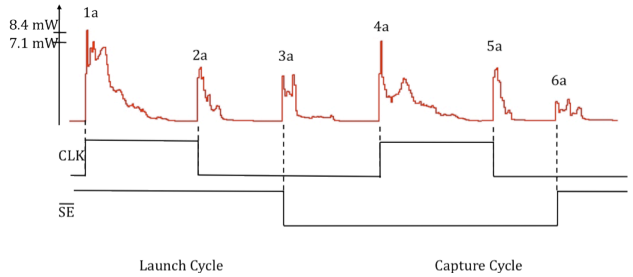

Figure 5: Transient analysis during LOS for b05

The detail of the contribution of the most meaningful peaks of LOS and LOC testing schemes is given below:

- *Peaks 1a and 1b*: Clock Tree switching (not considered); Scan Chain Flip-Flop switching (the slave part of FFs). These peaks are immediately followed by the switching activity of the combinational gates of the circuit. This activity reveals several peaks generally lower than 1a and 1b. Note that in this example, paths other than the critical paths (and hence with a shorter delay) have been sensitized. It may happen that in some cases (activation of critical delay paths), the switching activity after peaks 1a and 1b may last up to the end of the launch cycle, and hence is an additional contributor to peaks 2a, 2b and (for LOS only) 3a.

- *Peaks 2a and 2b*: Clock Tree switching (not considered); Scan Chain Flip-Flop switching (the master part of FFs). These peaks are followed by a limited switching activity that occurs in the scan chain(s).
- *Peak 3a*: Scan Multiplexers; Scan Enable tree; Scan Chain Flip-Flop switching (the master part of FFs). This peak, sometimes composed of multiple peaks (as in Figure 5), is always lower than the previous ones.

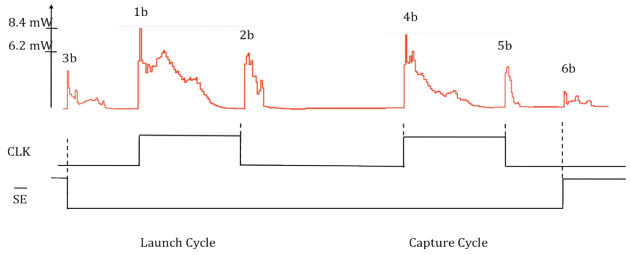

Figure 6: Transient analysis during LOC for b05

In both waveforms, the highest peaks of LOC and LOS (1a, 4a, 1b and 4b) are very similar in terms of amplitude. The main difference between the testing schemes is related to the scan enable signal switching during the launch cycle of LOS that causes a third peak in this cycle. The latter is not relevant in terms of peak power because it has smaller amplitude compared to the first two peaks. Conversely, it is important in terms of average power and is one of the causes of the larger cycle average power dissipated during the LOS launch cycle.

6. Discussion and Conclusions

First of all, it is important to mention that results on power consumption of LOS scheme have been obtained by considering conventional scan flip-flops for all circuits. No specific scan cell as those presented in [3,4] have been assumed, and hence power consumption due to extra logic has not be considered in our experiments. Nevertheless, it is shown in [4] that the area overhead and hence power consumption of the LTG (Last Transition Generator) cell used to generate a slow scan enable signal is negligible.

A first (predictable) conclusion shown by this study is that LOS scheme performs better than LOC scheme to detect transition faults. As LOC test can detect some faults not covered by LOS test and vice-versa, we have shown that a combination of LOS and LOC patterns is the best solution for achieving the highest TFC. A second (unpredicted) conclusion of this study is that peak power consumption of LOS test scheme is close and not far beyond the peak power consumption of LOC test scheme. A third conclusion is that although in the same order of magnitude than LOC, LOS power needs to be reduced i) during the launch-to-capture cycle and ii) during the first capture cycle when more than one capture cycles are used to test the CUT. From these statements, we can confirm the worth of LOS test scheme and the need to develop new solutions for reducing the test power of LOS in order to make it more attractive.

For this purpose, several methods can be investigated. As for LOC, new pattern-based and DfT-based methods can be defined. A straightforward solution to reduce LOS launch power is to use the adjacent-fill option during ATPG of LOS patterns. The adjacent-fill option has been shown to significantly reduce switching activity during LOS. However, the drawback is that TFC decreases and test length increases when using such option. Exploiting existing power management structures (e.g. clock gating) is another alternative to reduce LOS power. Several techniques based on this principle have been proposed in the literature for reducing LOC power [9] and could be exploited to deal with LOS power reduction.

References

[1] J. Savir, "Skew-Load Transition Test: Part I, Calculus", IEEE Int'l Test Conf., pp. 705-713, 1992.

[2] J. Savir and S. Patil, "Broad-Side Delay Test", IEEE Trans. on Computer-Aided-Design, Vol. 13, N° 8, pp. 1057-1064, 1994.

[3] G. Xu and A.D. Singh, "Low Cost Launch-on-Shift Delay Test with Slow Scan Enable", IEEE European Test Symp., pp. 9-14, 2006.

[4] N. Ahmed, C.P. Ravikumar, M. Tehranipoor and J. Plusquellic, "At-Speed Transition Fault Testing with Low Speed Scan Enable", IEEE VLSI Test Symp., pp. 42-47, 2005.

[5] K. Agarwal, S. Vooka, S. Ravi, R. Parekhji and A. Singh Gill, "Power Analysis and Reduction Techniques for Transition Fault Testing", IEEE Asian Test Symp., pp. 403-408, 2008.

[6] H. Furukawa, X. Wen, K. Miyase, Y. Yamato, S. Kajihara, P. Girard, L.T. Wang and M. Tehranipoor, "CTX: A Clock-Gating-Based Test Relaxation and X-Filling Scheme for Reducing Yield Loss Risk in At-Speed Scan Testing", IEEE Asian Test Symp., pp. 297-402, 2008.

[7] P. Girard, "Survey of Low-Power Testing of VLSI Circuits," IEEE Design & Test of Computers, Vol. 19, No. 3, pp. 82-92, May/June 2002.

[8] J. Saxena, K. M. Butler, V. B. Jayaram, S. Kundu, N. V. Arvind, P. Sreeprakash, and M. Hachinger, "A Case Study of IR-Drop in Structured At-Speed Testing", IEEE Int'l Test Conf., pp. 1098-1104, 2003.

[9] P. Girard, N. Nicolici and X. Wen (editors), Power-Aware Testing and Test Strategies for Low Power Devices, Springer, ISBN 978-1-4419-0927-5, 2009.

[10] K. M. Butler, J. Saxena, T. Fryars, G. Hetherington, A. Jain and J. Levis, "Minimizing Power Consumption in Scan Testing: Pattern Generation and DFT Techniques", IEEE Int'l Test Conf., pp. 355-364, 2004.

[11] P. Girard, X. Wen and N.A. Touba, "Low-Power Testing" in System-on-Chip Test Architectures: Nanometer Design for Testability, L.T. Wang, C.E. Stroud, and N.A. Touba (editors), Morgan Kaufmann Publishers, 2007, pp. 307-350.

[12] I. Park and E.J. McCluskey, "Launch-on-Shift-Capture Transition Tests", IEEE Int'l Test Conf., Paper 35.3, 2008.

[13] J. Abraham, U. Goel and A. Kumar, "Multi-Cycle Sensitizable Transition Delay Faults", IEEE VLSI Test Symp., pp. 6-, 2006.

[14] Z. Zhang, S. M. Reddy, I. Pomeranz, X. Lin and J. Rajski, "Scan Tests with Multiple Fault Activation Cycles for Delay Faults", IEEE VLSI Test Symp., pp. 343–348, 2006.

[15] Synopsys Inc., Design Compiler®, User Guide 2006.

[16] Synopsys Inc., PrimeTime®, User Guide 2006.

[17] Synopsys Inc., TetraMAX®, User Guide 2006.

[18] MentoGraphics, ModelSim®, http://www.model.com

[19] Synopsys Inc., NanoSim™, User Guide 2006.

[20] S. Remersaro, X. Lin, Z. Zhang, S.M. Reddy, I. Pomeranz and J. Rajski, "Preferred Fill: A Scalable Method to Reduce Capture Power for Scan Based Designs", IEEE. Int'l Test Conf., Paper 32.2, 2006.

[21] E.K. Moghaddam, J. Rajski, S.M. Reddy and M. Kassab, "At-Speed Scan Test with Low Power Activity", to appear in proc. of IEEE VLSI Test Symp., 2010.