Power-Safe Application of Transition Delay Fault Patterns Considering Current Limit during Wafer Test

Wei Zhao, Junxia Ma, Mohammad Tehranipoor
ECE Department
University of Connecticut
Storrs, CT, USA
{*wzhao, junxia, tehrani*}*@engr.uconn.edu*

Sreejit Chakravarty
LSI Corporation
Milpitas, CA, USA
sreejit.chakravarty@lsi.com

***Abstract*—Large switching during launch-to-capture cycle in delay test not only negatively impacts circuit performance causing overkill, but could also burn tester probes due to the excessive current they must drive. It is necessary to develop a quick and effective method to evaluate each pattern, identify high-power ones considering functional and tester probes' current limit and make the final pattern set power-safe. Compared with previous low-power methods that deal with scan structure modification or pattern filling techniques, the new proposed method takes into account layout information and resistance in power distribution network and can identify peak current among C4 power bumps. Post-processing steps replace power-unsafe patterns with low-power ones. The final pattern set provides considerable peak current reduction while fault coverage is maintained.**

***Keywords*-transition delay faults; low power test; flip-chip design; layout;**

I. Introduction

It is a well-known phenomenon that test power consumption exceeds that of functional operation in deep submicro designs. Due to the large capital costs imposed by test equipments, testers are usually behind the circuit speed and their power/current delivery remains almost same during their lifetime operation. Therefore, extensive switching in the circuit not only negatively impacts circuit performance, but could also result in tester probes burning due to excessive peak current drawn from it. It is vital to keep the test power/current under a limit that any possible damage to the tester can be avoided.

There are numerous existing low power test techniques to mitigate power issues, which can be mainly classified into two categories: 1. DFT-based solutions, which rely on modifications of scan structure, for example, scan clock blocking [1], scan chains segmentation [2], scan cells gating [3][4][5]; 2. ATPG-based solutions, which rely on analysis and adjustment of contents of delay test patterns, for example, different filling methods [6][7], primary inputs control [8], etc.

Nonetheless, we have observed in our experiments [9][10] that, the reduction of total switching activity, *1)* does not necessarily avoid high power consumption for a test pattern. *Weighted switching activity* (WSA) is a more effective metric to measure power consumption, as WSA considers the size of switching gates as well as their fan-out and load capacitance, which are necessary parameters for performing power analysis in digital designs; *2)* does not always avoid current spike or hot spot that appears in an specific region of the chip, since large switching can accumulate in a small area, and power supply around that area has to provide excessive current source for such switching activities. This can potentially damage tester probes connecting to the power pads in wire-bond designs or C4 bumps in flip-chip designs. Methods that are layout-aware, for example [9], have demonstrated effectiveness in detecting layout hot spots and peak currents.

Moreover, in spite of various low-power techniques adopted during either DFT or ATPG stage, there could still be some patterns that will cause high peak current in certain layout regions, since current ATPG methods are not layout-aware. As a result, *circuit under test* (CUT) and test equipment are still under the risk of experiencing power problems. It is necessary to grade test patterns based on power specifications of both CUT and tester. High power patterns need to be identified and replaced with low-power ones. During the pattern grading process, there should be no fault coverage loss in order to ensure test quality. Pattern count increment should be minimized to keep test cost in an acceptable range which depends on test time.

In this work, we focus on identifying peak current on C4 power bumps in the launch-to-capture cycle for flip-chip designs. We develop a layout-aware WSA metric to evaluate power behavior of each C4 power bump in order to identify largest peak current among all power bumps. Patterns are shortlisted based on bump current value. After pattern grading, a low power ATPG flow is adopted to create a new power-safe pattern set, which will have current below a pre-defined threshold, with pattern count increase in an acceptable range as well as little or no fault coverage

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loss. The proposed methodology can be easily integrated into existing ATPG/DFT flow, or can be used to identify peak current during scan shift process as well. Note that transistor level pattern simulation can accurately identify peak current on any node, but this process can be extremely slow especially for modern designs with a large pattern set, hence not feasible for practical use. The layout-aware WSA flow proposed in this work is based on logic simulation with zero delay, making it applicable for large designs.

The remainder of the paper is organized as follows. Section II introduces power model and current limitation for tester probe. Section III describes our methods of layout partitioning, resistance network construction and power bump WSA calculation. Section IV presents the integrated methodology for pattern grading, selection and final power-safe pattern generation. In Section V, experimental results and analysis are presented. Finally, the concluding remarks are given in Section VI.

II. Preliminaries

A. Power Model

To simplify the measurement of dynamic power consumption in this work, *weighted switching activity* (WSA) [3] is used to represent power and current within the circuit, as represented by Equation (1) [9][11].

$$WSA_{gk} = d_k(\tau_k + \phi_k f_k), \text{ where}$$
$$d_k = \begin{cases} 1, & \text{Transition occurs} \\ 0, & \text{No transition} \end{cases} \quad (1)$$

For gate k, the WSA_{gk} will be dependent on the gate weight τ_k, the number of fan-outs of the gate f_k, and the fan-out load weight ϕ_k. The WSA sum for the entire circuit WSA_C with n gates can be expressed by Equation (2). Similarly, the number of gates n can be replaced with any other number of gates in the circuit, for example, instances in a specific layout region as described in the next section that deals with layout partition.

$$WSA_C = \sum_{k=1}^{n} WSA_{gk} \quad (2)$$

Since peak current is proportional to peak power consumption, and WSA is a representation of current, the peak current or power issues in test patterns can be transformed to the analysis of pattern WSA. We use the reduction of peak WSA to represent the reduction of peak current in this work.

B. Current Limitations

A large array of C4 bumps are needed to supply the necessary current for the chip to operate since a single C4 contact may only provide an average of 50mA of current delivery to the chip [12]. This becomes a problem in wafer-level testing, where probe needles deliver the power to the chip. As Figure 1 shows, with technology scaling, the allowable current during wafer test falls behind functional operation

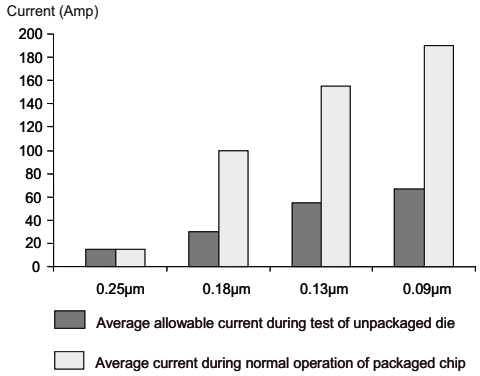


Figure 1. Power availability during wafer testing [12].

of packaged chips, in which many chips today already consume >>50A of current. Designing probe cards with thousands of probe contacts may not only be achievable, but also introduce significant inductance (Ldi/dt) [12][13] which increases power supply noise. Consequently, in order to ensure power safety during wafer delay test, it is necessary not only to be aware of functional power limitation of CUT, but also current limitations of tester probes. Peak test current during pattern application should not surpass either of the limit. We believe this work is the first to consider current limitations of tester probes.

A WSA threshold WSA_{thr} is used in this work to represent safe current for both CUT and tester probes, the value of which is determined as follows: firstly, a current limit I_{thr} is obtained considering both CUT functional limit I_{func} and tester probe limit I_p, Then, the relationship between WSA and current can be studied through sample pattern simulation and silicon test. With the knowledge of coefficient between WSA and current values, we obtain a value WSA_{thr} corresponding to the required I_{thr}. A small margin can be added to this threshold for conservative testing regarding peak current issue. At this point, we do not have access to such data, therefore, we set a reasonable WSA_{thr} based on circuit functional limit and assuming that the tester current limit is comparable to functional limit. Note that, we will be implementing this technique on LSI designs and collect data on silicon to perform correlation analysis between WSA_{thr} and tester probe's current limit. In this work, we set $WSA_{thr} = 30\%$, which indicates 30% of original patterns have peak current above threshold.

III. Layout Partitioning and C4 Bump WSA Calculation

In order to avoid peak current above limit on a C4 power bump, it is necessary to monitor current or power behavior on each bump instead of considering solely the power consumption for the entire chip, since there is a chance that the total power consumed is within the limit of specification, yet on one power bump, the current required is beyond its

capability, thus the excessive current flowing through that bump can cause damage to the circuit underneath the bump area as well as tester probe connecting to that bump. Here, we propose the concept of *bump WSA* (WSA_B) as a metric to measure the current strength on a single power bump, *peak bump WSA* (WSA_{BP}) to represent the peak current among all power bumps, and *average bump WSA* (WSA_{BA}) to represent the average WSA_B for all power bumps. In this work, all measurements are performed regarding the launch-to-capture cycle.

In order to measure WSA_B, two sets of data should be ready: *1)* WSA_{gk}, which is the weighted switching activity of each gate in the CUT; *2) bump location*, which structurally shows how a bump provides current to the gates through the power distribution network. Descriptions for 1) are presented in Subsection (III-A), in which we describe how transition is monitored and WSA calculated. Discussions related to 2) are arranged in Subsection (III-B), in which we demonstrate layout partitions based on power distribution network and calculate regional WSA. In Subsection (III-C), a resistance network is constructed based on layout partitions and bump locations, which is combined with WSA data to finally obtain WSA_B for each C4 power bump.

A. Transition Monitoring

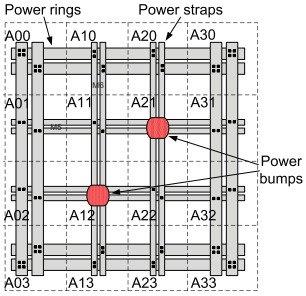
We use logic simulation to monitor transitions. The Verilog *programming language interface* (PLI) subroutines are utilized to monitor which gates switched during the launch-to-capture cycle. Zero-delay is used. Transition arrival times are not considered. Only the final rising or falling transitions are recorded and any glitches during the launch or capture window are ignored at this point. We will take glitches into account in future work.

As Equation (1) shows, both the weight of a switching gate and its fan-out can affect a WSA_{gk} value hence the current strength. The PLI routine is used here again to look up the weight of each switching gate, as well as to determine the number of its fan-outs. After acquiring all these information, the PLI routine is able to report WSA of each switching gate, WSA_{gk}.

B. Layout-Aware Profiling

In order to locate transitions in the circuit, layout information is needed to identify the location of each gate. Standard *design exchange format* (DEF) file is used to extract gate coordinates, as well as the power supply network. A two-dimensional array (matrix) can be overlaid on top of the layout that divides it into smaller partitions.

Figure 2(a) illustrates how a physical design is divided into smaller regions based on the power supply network. In this example, there are two straps vertically across the chip in *Metal 6* (M6), two horizontally across the chip in *Metal 5* (M5), and power/ground rings around the periphery of the design. Using the straps as midpoints for each region in the matrix, the chip is then divided into four columns and four rows for a total of sixteen (16) regions. Two power bumps are located above the regions of A_{12} and A_{21} (A here stands for each area or region), connecting to two separate power straps respectively. In this work, the size of region matrix is $(N+2) \times (N+2)$, where N is the number of vertical straps on M6. In Figure 2(a), there are $N = 2$ vertical power straps, therefore the region matrix size is 4×4.



(a)

A_{00} 526	A_{10} 318	A_{20} 223	A_{30} 0
A_{01} 474	A_{11} 590	A_{21} 602	A_{31} 345
A_{02} 351	A_{12} 379	A_{22} 425	A_{32} 293
A_{03} 187	A_{13} 253	A_{23} 187	A_{33} 150

(b)

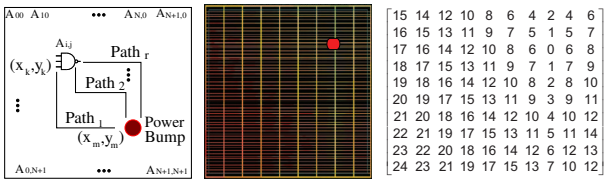
Figure 2. Layout partitions: (a) An example of the power straps being used to partition the layout into regions. (b) An example of WSA_A matrix.

The partition matrix only needs to be created once for each design. When a switching is detected, the location of the switching instance is looked up and mapped to a region in the matrix, say A_{ij}, then a WSA_{gk} calculated using Equation (1) for that instance is added to this region A_{ij}. When simulation ends, each region is filled with a sum of WSA_{gk}, which is all the transition events that have occurred in that region. We define WSA which is related to each region as WSA_A. In this work, for example, when applying a delay test pattern, all regions have WSA_A initialized to 0 at the beginning of launch-to-capture cycle. When this cycle ends, the partition matrix has a one-to-one mapped $WSA_{A_{ij}}$ as shown in Figure 2(b). Note that, a region with a 0 value ($WSA_{A_{ij}} = 0$) in the matrix implies no switching in the region or even no instance placement in it. This could potentially happen in some peripheral regions.

C. Bump WSA Calculation

The power bumps are connected to the highest level metal over the core area. The highest level metal dominates current flow. That is, the power source, in wafer test provided by tester probes, is distributed from high level metals to low level ones, then eventually to the power pins of the gates. To obtain current from supply, a switching gate in a region is likely to draw more current from its nearby power bumps [14]. In other words, those further-away bumps contribute less to providing current to the switching gate. Similarly, considering a specific region as a whole, the ratio of current drawn from different bumps is inversely proportional to the distances from region to bump locations, which can be characterized by the resistive path between these two objects, as shown in Figure 3(a). The layout is divided into regions

labeled from A_{00} to $A_{(N+1)(N+1)}$. A power bump is placed over the right bottom of the core, with coordinates (x_m, y_m). Suppose a switching gate with coordinates (x_k, y_k), located at A_{ij} has r number of paths reaching the bump through power network. The resistance from the gate (or region) to that bump can be calculated by Equation (3). $g_{A_{ij}->B_m}$ is the conductance from region A_{ij} to bump B_m. g_{path_q} is the conductance on one power path from A_{ij} to B_m.



(a) (b) (c)

Figure 3. Resistance path and resistance network: (a) Resistance paths from an instance or region to a power bump; (b) least resistance plot from SOC Encounter for a specific power bump; (c) least resistance network.

$$g_{A_{ij}->B_m} = \sum_{q=1}^{r} g_{path_q}$$
$$R_{A_{ij}->B_m} = \frac{1}{g_{A_{ij}->B_m}} \quad (3)$$

To make computation easier, which is based on the fact that these resistive paths are in parallel, we can simply consider the *least resistance path* (LRP), thus Equation (3) is reduced to be Equation (4).

$$g_{A_{ij}->B_m} = g_{LRP} = min\{g_{path_1}, g_{path_2}, ..., g_{path_r}\} \quad (4)$$

Figure 3(b) shows least resistance plot in Cadence SOC Encounter when there is a power bump on a top-right region. The color is plotted based on the rule that regions with smaller resistance to the power supply are drawn in brighter color. Therefore, the brightest color is observed around the beneath of power bump since these regions have smallest path resistance to the power supply. Darkest plot appears in bottom-left regions since they have largest path resistance to the supply. Figure 3(c) presents the resistance matrix (unit Ohm) constructed based on bump location in (b). Each region in the 10×10 resistance matrix is assigned a value based on its distance to the power bump. The region that have bump directly above its area is assigned the smallest resistance value, 0, in this example, which corresponds to the brightest region in (b). The farther a region is from the bump, the larger *R* value is assigned to that region. The maximum value appears at the left bottom region of the matrix, which corresponds to the darkest region in (b). In our procedure, we use Equation (4) to obtain a resistance value for each region. We maintain a separate resistance network for each power bump. Below we provide the method of calculating WSA_B.

Suppose there are $(N+2) \times (N+2)$ regions, M power bumps, and we have already obtained WSA_A for all regions

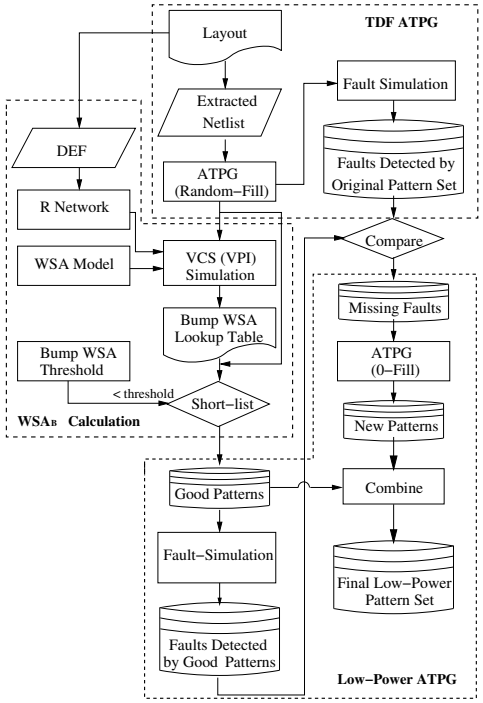


Figure 4. Flow diagram of pattern grading and power-safe pattern generation.

through transition monitoring, the WSA sum for a specific power bump is calculated by Equation (5). In this equation, WSA_{B_m} is the WSA for power bump m, which represents total current drawn from this bump. $WSA_{A_{ij}}$ is the WSA sum for region A_{ij}. This equation can be understood as this: the WSA on a power bump draws a portion of WSA from each region. The percentage for this portion is determined by that region's resistive path to all power bumps. The detailed discussion for WSA_B calculation is presented in *step 2* in Section IV.

$$WSA_{B_m} = \sum_{i=0}^{N+1} \sum_{j=0}^{N+1} \frac{g_{A_{ij}->B_m}}{\sum_{q=1}^{M} g_{A_{ij}->B_q}} \cdot WSA_{A_{ij}} \quad (5)$$

IV. Pattern Grading and Low Power Pattern Generation Flow

The layout-aware power-safe pattern generation procedure integrates bump WSA calculation introduced in Section III with the existing commercial ATPG tools to prevent patterns from excessively exceeding maximum allowable current. This will also prevent patterns from over exercising the chip beyond functional stress. The pattern grading flow is shown in Figure 4, which can be divided into three main steps: 1) TDF ATPG, 2) WSA_B calculation, and 3) low-power ATPG.

• *Step 1. TDF ATPG*: The first step in the flow involves conventional TDF ATPG with any commercial tool. In this

step, layout information is ready for extracting both netlist and DEF files. The netlist is then fed to ATPG tools for generating TDF test patterns, which is called original pattern set in this work. This pattern set is then passed to fault simulator to determine detected faults and fault-coverage. Note that, we use random-fill in ATPG to minimize pattern count.

• *Step 2. WSA_B Calculation*: The second step aims to construct a WSA_B lookup table, with row corresponding to different patterns while column for different power bumps. Each element in this table is a WSA_B value that associates with a bump and pattern. To construct such a table, firstly, zero-delay logic simulation is performed to monitor switching events in each pattern. As only launch-to-capture cycle is considered, we use parallel pattern simulation instead of serial to save a great deal of computation time, especially for large designs. More specifically, at the beginning, the coordinates of all gates, power rings/straps and bumps are extracted from DEF file. During simulation, WSA_{gk} is calculated for each switching gate using Equation (1), which is then mapped and added to a $WSA_{A_{ij}}$ value that associates with a layout region containing the gate. Thus, a WSA_A matrix can be obtained after a pattern simulation is finished. Each power bump has a same-size resistance network with layout partition or WSA_A matrix, as illustrated in Figure 3(b) and 3(c). Each cell in resistance network is based on its LRP to that bump. If there are M power bumps, M resistance networks need to be created respectively. Then $WSA_{A_{ij}}$ is divided into M portions based on its LRP ratio to all power bumps. We understand that each power bump provides a part of its WSA/current to all regions. Thus WSA_B is obtained accumulatively using Equation (5). This process is iterated for all patterns. The WSA_B lookup table can be constructed when parallel pattern simulation finishes. In the table, each pattern has M WSA_B values, the maximum among which, WSA_{BP}, represents peak current for that pattern.

• *Step 3. Low-Power TDF ATPG*: After WSA_{thr} is applied, patterns with maximum WSA_{BP} higher than this threshold will be removed. The short-listed patterns are called *good patterns* in our flow. Fault simulation is done on *good patterns* to get detected faults, which will be compared with the *detected* faults of original pattern set to determine the *missing faults*. In order to maintain fault coverage, some *new patterns* are generated by ATPG tool trying to cover the *missing faults* with 0-fill scheme. However, any of existing ATPG-based low-power techniques can be used in this stage, for example, the aforementioned [6][7][8]. The *new patterns*, combined with *good patterns* form a final low-power pattern set.

V. Experiment Results

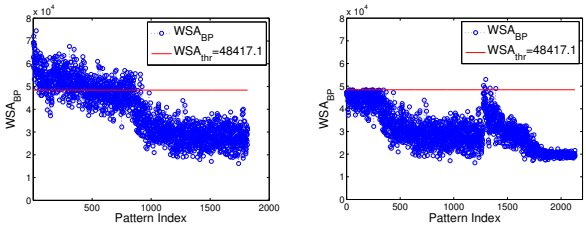
The layout-aware power-safe delay test pattern generation flow was implemented on Linux-based x86 architectures with 3GHz processors and 32GB of RAM. The gate netlists were physically synthesized using Cadence SOC Encounter. TDF patterns were generated using Synopsys TetraMax. Pattern simulation was performed with Synopsys VCS with the PLI procedures implemented in C. Pattern short-listing and new pattern generation were integrated into TetraMax Tcl scripting environment.

Table I
Benchmarks characteristics.

Benchmark	# of Gates	Total Faults	# of Straps	WSA Matrix Size
s9234	3712	4910	2	16
s38417	38536	47182	2	16
b19	284319	474160	2	16

The flow was tested on three benchmarks with different size that are listed in the Table I. The original pattern set in TDF ATPG stage is generated using random-fill, and low-power ATPG using 0-fill. Results of these three benchmarks are listed in Table II. In this experiment, we set $WSA_{thr} = 30\%$, which indicates that 30% of original patterns are regarded as power-unsafe and will be discarded during short-listing.

In Table II, WSA_{BP} represents peak bump WSA for all patterns. WSA_{BA} is the average bump WSA. The result shows that as benchmark size increases, our pattern grading flow performed more effectively in reducing their WSA_{BP}. For example, WSA_{BP} in the smaller benchmark s9234 decreased by *7.4%*, while for benchmark b19, it decreased by *28.9%*. The same reduction trend is observed for WSA_{BA}. However, pattern count increased more in b19 than s9234, *17.2%* for b19 compared to *4.8%* for s9234. Test pattern count increase can be regarded as a trade-off with WSA_{BP} reduction in this flow. Figures 5(a) and 5(b) show WSA_{BP} plots for b19 original pattern set and final low-power pattern set respectively. Figure 5(a) shows there are 544 out of 1817 patterns that are above WSA_{thr}, while only 6 patterns in the final pattern set in Figure 5(b).



(a) (b)

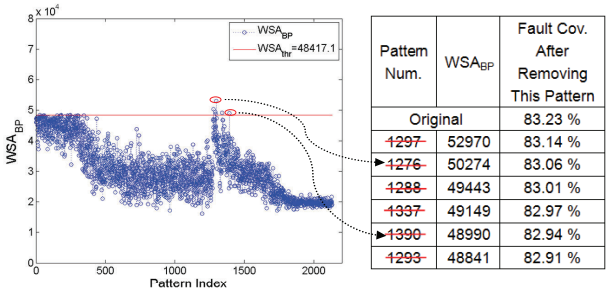
Figure 5. WSA plot for b19 benchmark: (a) original pattern set; (b) final low-power pattern set

A. Further Reduction of Peak WSA

There could still be some patterns with WSA_{BP} above WSA_{thr} in the pattern set. Figure 5(b) shows six such patterns. There are two methods to solve his, so as to make WSA of final pattern set completely below WSA_{thr}. One method is to remove these patterns from final set if there are only few. Figure 6 shows fault coverage results by removing six patterns one by one, with the coverage value decreasing from *83.23%* to *82.91%*.

Table II
COMPARISON BETWEEN ORIGINAL PATTERN SET AND FINAL PATTERN SET, $WSA_{thr} = 30\%$.

Bench-mark	Original Pattern Set				Final Pattern Set				Difference		
	# of Patt.	Fault Cov. %	WSA_{BP}	WSA_{BA}	# of Patt.	Fault Cov. %	WSA_{BP}	WSA_{BA}	Δ Patt. %	Δ WSA_{BP} %	Δ WSA_{BA} %
s9234	167	85.60	754	448	175	85.52	698	390	$\uparrow$ 4.8	$\downarrow$ 7.4	$\downarrow$ 12.9
s38417	180	94.72	6642	4936	190	94.72	5415	4303	$\uparrow$ 12.5	$\downarrow$ 18.5	$\downarrow$ 12.8
b19	1817	83.26	74482	37666	2129	83.23	52969	28764	$\uparrow$ 17.2	$\downarrow$ 28.9	$\downarrow$ 23.6



Pattern Num.	WSA_{BP}	Fault Cov. After Removing This Pattern
Original		83.23 %
~~1297~~	52970	83.14 %
~~1276~~	50274	83.06 %
~~1288~~	49443	83.01 %
~~1337~~	49149	82.97 %
~~1390~~	48990	82.94 %
~~1293~~	48841	82.91 %

Figure 6. Fault coverage loss analysis for b19 benchmark when removing the remaining high-power patterns from the pattern set.

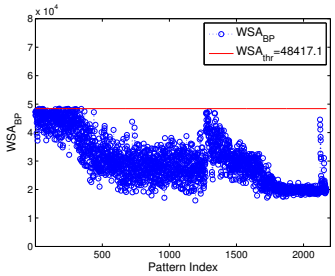


Figure 7. WSA plot for final pattern set after second round for b19 benchmark.

The other method is to run the flow for two or more rounds. In other words, use the final pattern set obtained in the first run as the original pattern set in the second run. In this experiment, we used pattern set shown in Figure 5(b) as original pattern, for which the WSA plot for the second round is shown in Figure 7. For the second round, no patterns were above WSA threshold any more. In this round, 42 new low power patterns were generated to make up the fault coverage loss by removing 6 high power patterns in the first round. Thus, this method took additional CPU run time to obtain final pattern set for the second round. However, we only need to run WSA analysis for these 42 new patterns, thus CPU run time increase is small, e.g. 13 minutes for b19.

VI. CONCLUSIONS

We have presented a novel layout-aware power-safe TDF pattern generation flow, which targets flip-chip designs considering its functional power limit as well as current limit on tester probes. The goal of our flow is to ensure that the final TDF pattern set is power-safe for both CUT and test equipment. The flow requires a WSA threshold to be predefined based on the desired power limit. Then we calculate WSA of power bumps for each pattern. In this step, the layout is analyzed and partitioned into small regions. WSA for each region is obtained and used to determine power bump WSA based on bump locations. Any patterns from original pattern set that have bump WSA above the threshold will be considered as power-unsafe and discarded. New low-power patterns are generated to make up the fault coverage loss. Our experiments show that for the b19 benchmark, the peak WSA of the final pattern set obtained from our flow can be reduced by 29%, with 17% pattern count increase and almost no fault coverage loss. The flow can be can be easily integrated with commercial and industrial flows.

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