Emulating and Diagnosing IR-Drop by Using Dynamic SDF

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Abstract

The Standard Delay Format (SDF) information is very important in timing-aware simulation of VLSI designs. However, conventionally, SDF is only design-dependent, but pattern-independent, which is called static SDF in this paper. Static SDF ignores all dynamic pattern dependent parameters, such as IR drop and crosstalk. In this paper, we propose a novel pattern-dependent SDF (called dynamic SDF) generation technique, and apply it to take IR-drop effects into consideration. With the proposed IR-drop-aware SDF generation technique, we improve the accuracy of simulation, and perform diagnosis on the failed patterns to pin point the pattern-dependent IR-drop defects in our design. Experimental results demonstrate the efficiency of this method when used for transition delay fault pattern application and diagnosis.

1. Introduction

Timing-aware simulation is a very important technique for analyzing the specifications of VLSI designs. It can help to validate the behavior of a design and its test patterns [1]. Several simulation techniques were proposed for circuit simulation and analysis. The Simulation Program with Integrated Circuit Emphasis (SPICE) [2] is the most trustable and comprehensive analog circuit simulator in industry and is often used as a "gold standard". Unfortunately, due to its computation complexity, SPICE is incapable of dealing with the simulations on the entire design with millions of gates. Gate-level netlist simulation with SDF (Standard Delay Format) annotation is widely used for logic and timing verification of the designs [3]. For this kind of simulation, a test-bench is built to provide stimuli, and to check the response of the design. The timing information of each gate and interconnect of the design, which were extracted from a standard library, is annotated to the design during simulation for performance analysis and evaluation. The SDF-based digital simulation is a much faster approach than SPICE for design analysis and verification, and is easy to be scaled up for large designs. However, the conventional SDF file for a design comes from Static Timing Analysis (STA) and is pattern-independent thus is incapable of reflecting some pattern-dependent parasitic effects (also known as environmental variations), such as IR drop and crosstalk. In this paper, the conventional pattern-independent SDF is called static SDF. Although there are min/typical/max delay values for best/typical/worst cases in the static SDF, it may still not be able to reflect the real situation accurately without considering test patterns.

With the VLSI technologies scale down to nanometers, the impact of pattern-dependent parasitic effects such as IR drop and crosstalk must be considered during both design and test. Nanometer technology allows packing more transistors into one chip and increasing the operating frequency of transistors, which in turn results in increased switching and power density. Furthermore, the power supply voltage is scaled down for reducing leakage current. However, the reduced power supply voltage also compromises the noise immunity impacting signal integrity of the design. The impact of power supply noise on gate delays becomes increasingly significant as technology and power supply voltage scales [4] [5] [6] [7].

The impact of power supply noise on gates and circuit performance has been addressed in several prior works. The authors in [6] proposed an ATPG method to generate path delay test patterns maximizing power supply noise effects. In [16] and [17], the authors proposed supply voltage noise aware ATPGs for minimizing the power supply noise effects on path delays. In [18], the authors presented a pattern compaction technique for IR-drop tolerant transition delay fault (TDF) pattern generation. In [19], statistical analysis is applied to evaluate the IR-drop effect on path delays. The authors in [8] proposed power noise models for array-bond and wire-bond chips for delay testing. Their models are used to compact test vectors while meeting noise and delay constraints. A look-up table is built in [9] for computing the propagation delay of the target paths under power supply noise effect. However, this model assumed linear relationship between delay and voltage, which does not seem accurate. Most of the previous works are about IR-drop modeling or IR-drop-aware pattern generation rather than IR-drop defects diagnosis.

In this paper, we propose a novel flow using dynamic SDF to model IR drop. The flow allows a fast and accurate IR-drop-aware digital simulation for verifying design specifications and test patterns. It can also be used to diagnose IR-drop-induced defects by reporting the gates that experience severe IR-drop and delay increase and improving the diagnosis resolution for IR-drop-caused failures. The remainder of this paper is organized as follows. Section 2 presents the IR-drop analysis flow. Section 3 introduces accurate modeling of IR-drop effects.

978-1-4244-5766-3/10/$26.00 ©2010 IEEE

In Section 4, we perform diagnosis to validate the failure paths and to pin point key gates for IR-drop failures. Experimental results are presented in Section 5, followed by the conclusions and discussions on the future work in Section 6.

2. IR-drop Analysis

The circuit density and operating frequency of current VLSI designs increase as technology scales leads to severe power density problem. Power supply noise can be introduced by inductive and resistive parameters. The inductance-introduced noise, usually referred as *Ldi/dt*, depends on the changing rate of instantaneous current flowing through the power distribution network (PDN), as well as the inductance *L*, which is mainly introduced by packaging. The resistance-introduced noise, usually referred as IR drop, depends on the current and distributed resistance on the PDN. In this work, we only focus on the resistance-introduced power supply noise and their impacts on the design performance.

Figure 1 shows a simplified PDN for a standard-cell based design. In this design, standard cells are placed side-by-side in rows. Local power rails between standard cell rows are formed in lower metal layer (Metal 1 or Metal 2, depending on the design cells in the library). The global power rails are always routed in upper metal layer. Power vias are used to connect the global and local power rails. When there are switching activities on the cells, they will either draw current from the power rails (for charging the output nodes and capacitors) or dump current to the ground rails (for discharging the output nodes). Due to the resistance on the PDN, the current will result in a voltage drop on the power network and/or a voltage increase (also known as ground bound) on the ground network. For simplicity, only the voltage drop on power network is considered in this paper. However, it would be easy to add the voltage increase on ground network to the procedure by using the same proposed flow.

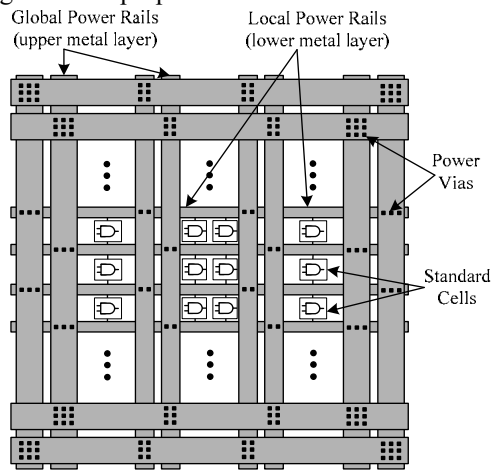


Figure 1. A simplified view of PDN

In the first step of IR-drop analysis, we run ATPG to generate at-speed patterns targeting TDFs. For each TDF pattern, we run simulation to get its value change dump (VCD) file, with which we perform IR-drop analysis using a commercial EDA tool [11] and get the average IR-drop in a specified timing window of each gate in the design. The specified timing window for each at-speed pattern is within the launch and capture clock cycles.

Note that the real voltage value on a specific gate is dynamic during launch and capture window. Figure 2 illustrates an example of the real voltage value between the launch and capture cycles on one gate in our experiment. The IR-drop analysis tool can only report the average voltage drop of gates in a user-defined timing window. Therefore, the timing window for IR-drop analysis should be carefully selected to make sure that the IR-drop results can accurately reflect the real situation in terms of performance impact. Our timing window for IR-drop analysis starts at the launch clock cycle. The end point of a timing window is chosen based on SPICE simulation to make sure that the average IR-drop induced delay and the real dynamic IR-drop induced delay are as close as possible. Hence, the average IR-drop can be used to evaluate the extra delay on each gate and interconnect in the design.

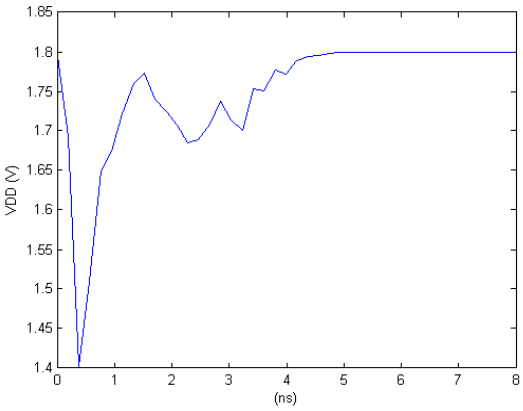


Figure 2. Dynamic IR-drop on a gate during the launch and capture cycles

3. IR-Drop and Extra Delay Database

In this section, we introduce building up IR-to-delay database (named IR2Delay database in our experiments) to map the average power voltage drop to the delay increase for all cell models in the design library based on SPICE simulation. Mentor Graphics Eldo is used for SPICE simulation [13]. An in-house tool was developed to automatically extract gate SPICE models from the library, set up test circuits, run simulation and extract the simulation results.

3.1 Transition Analysis

For each cell model in the library, we will measure its delay from all its inputs to its output for both rising and falling transitions. Clearly, when the cell has multiple input pins, there should be a transition on this targeted input pin when measuring the propagation delay from it to the output of the cell. All the other input pins, which are called *off-path pins*, must have non-controlling values such that the transition on the targeted input pin can be propagated to the output. Furthermore, the status of off-path pins may impact the results. Consider a 2-input AND gate as an example. As illustrated in Figure 3, a total of seven cases should be considered when we measure the rising edge propagation delay from the input pin A to the output pin Y. The propagation delay of all these cases are measured via SPICE simulation and listed in Table 1. It is easy to measure the delay in case (1) when off-path pin B is stable. If off-path pin B has a rising transition and its transition arrives earlier than the transition on pin A, as shown in case (2), pin B is stable when the transition on pin A arrived, which is the same as case (1). Similarly, for case (3), the output transition is determined by the transition on pin B, and Pin A should be considered as off-path pin. For instance, due to a 2ns difference between the A and B transitions, we obtain a 2.1320ns delay from pin A to pin Y.

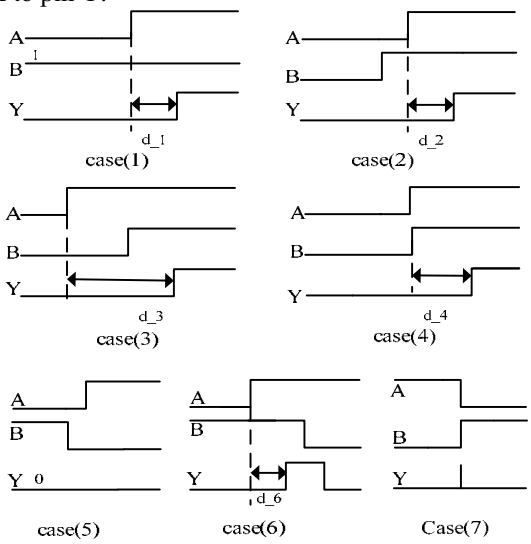


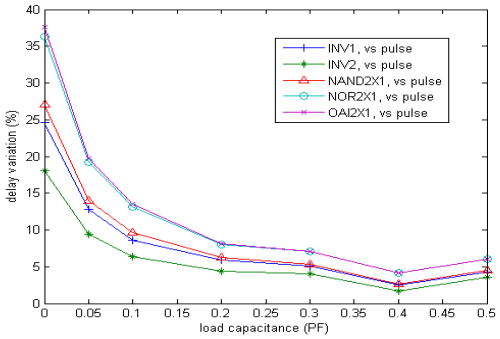
Figure 3. Rising edge transition propagation of an AND2X1 gate

Table 1. Propagation delay from A to Y for an AND2X1 gate (load capacitance: 50FF)

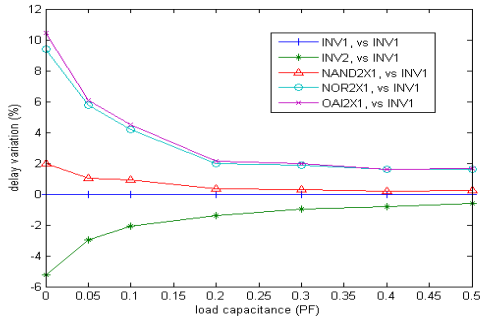
Test case	Case (1)	Case (2)	Case (3)	Case (4)	Case (5)	Case (6)	Case (7)
delay (ns)	0.1288	0.1288	2.132	0.1371	—	0.1288	—

When pin B has a rising transition simultaneously with pin A, as shown in case (4), it impacts the propagation delay on pin A. From Table 1 we can see that the delay increased is about 6.4% compared with case (1) or (2). When pin B has a falling transition, case (5) or (7) should not be considered since they cannot ensure the transition on pin A can be propagated to the output pin Y. In other words, the falling transition on pin B has to arrive later than pin A's transition, as shown in case (6). In this case, the rising transition propagation delay from A to Y is also the same as what we experience in case (1). In summary, the rising edge propagation delay from pin A to pin Y can be measured by setting pin B to 1 as shown in case (1). Although the simultaneous transitions (e.g. case (4)) will impact the propagation delay, we can ignore it since the delay variation is small (6.4% in our experiments). The same can be applied to the falling transition propagation delay. In this paper, all off-path pins are set to non-controlling values when measuring the propagation delay from one input pin to the output.

3.2. Driving Strength Analysis



(a)



(b)

Figure 4. Delay variations of BUFX3 gate when driven by (a) different logic gates vs. pulse source driver and (b) different logic gates vs. INVX1 gate

In any design, a non-primary input (PI) gate is driven by another gate with finite driving strength. A non-PI gate is a gate that none of its inputs is directly connected to a PI. The driving strength of the driving gate can also impact the propagation delay on the targeted driven gate. Consider a buffer cell (BUFX3) as an example. Figure 4 shows the delay variations between the driving gates vs. pulse source (a) and the delay variations between the

driving gates vs. INV1 gate (b), with different output load capacitance of the targeted driven gate. The pulse source in this paper refers to the ideal pulse signal with infinite driving strength in SPICE simulator.

From the above figures, we can see that with the increase in load capacitance, the delay variations of different driving gates would be reduced. Regardless of the output load capacitance, the delay variation between gate driver and pulse source driver is significantly larger than the delay variation between various gate drivers and INV1 gate driver. Therefore it is more accurate to drive the targeted driven gate with a logic gate, rather than with a pulse source, when measuring its gate delay. These delays may vary for different driving gates, but the variation is small and hence can be ignored to simplify and speed up the procedure. In our experiments, we select an appropriate driving gate to drive the targeted gates when measuring their delays. The appropriate driving gate is a gate with sufficient driving strength to drive the test gate.

3.3. Power Voltage-Delay Map

An in-house tool was developed to perform SPICE simulation and set up the power supply voltage-delay map. For each cell model in the library, we run SPICE simulations and measure its propagation delays with

- different propagation paths, from all input pins to the output pin;
- different transition direction, including rising and falling transitions;
- different power voltage;
- different load capacitance.

As mentioned in subsection 3.1, when measuring the propagation delay from one input pin to the output pin, the off-path pins are kept to be stable non-controlling values. The logic gate with proper driving strength is selected to drive the targeted gate as discussed in subsection 3.2.

The simulation results are written into an IR2Delay database to be used for generating dynamic SDF later. Generally speaking, a large IR-drop will result in a large delay increase. However, for different gates, the same IR-drop will result in different extra delay. The relationship between IR-drop and delay increase of all cells are reflected in the IR2Delay database.

4. Diagnosis for Failure Paths

Whether an at-speed test pattern can fail on tester depends on the real delay of gates and interconnects in silicon, as well as the test clock frequency, if there is no physical defect (e.g. resistive open defect) in the design. For our TDF test patterns, we run simulation and select an at-speed frequency based on the critical path delay to make sure that there are no failures with the original static SDF file of the design. Then we quickly generate dynamic SDF file for each pattern with IR-drop effect and rerun simulation again. If we push the operating clock frequency to its limit, it can be seen that some patterns fail with the dynamic SDF files. In this controlled experiment, the IR-drop
effect is the only reason for the failures. Then we run commercial diagnosis tool [15] to report the suspect failure paths.

The diagnosis tool will check the failed bits in the failure log, with which to back trace the design. Logic simulation is run to see which paths may potentially fail the target bits. However, for a specific target failed bit, there may be several logic paths that could fail it. Without accurate timing calculation, the tool could not tell which path is exactly the cause of the target failed bit. Thus, it just reports all the possible paths as suspect failure paths.

With the dynamic SDF, we can do accurate timing analysis on the suspect failure paths to see which paths do violate the timing constrains of the design, and hence to improve the resolution of current diagnosis tool. We can also compare the timings in the dynamic SDF and original static SDF to see which gate(s) are the major cause of the timing failure so that can exactly pin-point the failure gate(s) in the design, which also is an improvement to the diagnosis resolution.

5. Experimental Results

The entire flow is illustrated in Figure 5. The flow was verified on the IWLS benchmark ac97_ctrl, which contains 9,656 logic gates and 2,199 flip-flops. We use 180nm Cadence Generic Standard Cell Library with typical 1.8 V power supply voltage. Synopsys Design Compiler [10] was used for logic synthesis. Cadence SoC Encounter [11] was used for layout placement and routing, as well as IR-drop analysis. Mentor Graphics FastScan [12] was used for pattern generation. Mentor Graphics Eldo [13] and ModelSim [14] were used for SPICE simulation and digital simulation, respectively. Mentor Graphics YieldAssist [15] was used for diagnosis. The power supply voltage-delay map procedure was implemented with Perl, and the SDF Updater and post-diagnosis timing analysis tool were implemented in C/C++.

For a specific test pattern, the IR-drop analysis flow can report the average power voltage of each gate in the design. Combined with load capacitance information extracted from layout and transition direction from the pattern, from the IR2Delay database we obtain the rising or falling delay increases for each gate, from all input pins to its output pin. The SDF Updater (see Figure 5) can update the gate and interconnect delays in the original static SDF file. Therefore for each pattern, we can dynamically produce a new SDF file (also called dynamic SDF file). Table 2 shows the power voltage and delay profiles of several sample gates in our experimental benchmark, for a specific test pattern. The “original” delays in this table are extracted from the original static SDF file of the design without considering IR-drop effect,

while the "updated" delays are extracted from the updated SDF file for the test pattern with IR-drop consideration. It can be seen from the last row of the table that the delays of some gates increase significantly due to the IR-drop effect (for example, gate U8701 has over 18% extra delay). Therefore, it is necessary to take the IR-drop effect into consideration for accurate performance evaluation. Furthermore, unlike common belief that the delay of a gate always increases with IR-drop impact, our experiments demonstrate that sometimes for a specific transition direction, the delay of a gate may decrease due to the IR-drop effect (see the 1->0 delay of gate U12160). This is because the output of the gate has a lower VDD. When there is a falling transition at the output pin of the gate, it is faster to discharge from the output pin. However, if we calculate the total delay change for a path, the delay may still increase. In a word, it will overestimate the design performance if analyzed with the original static SDF.

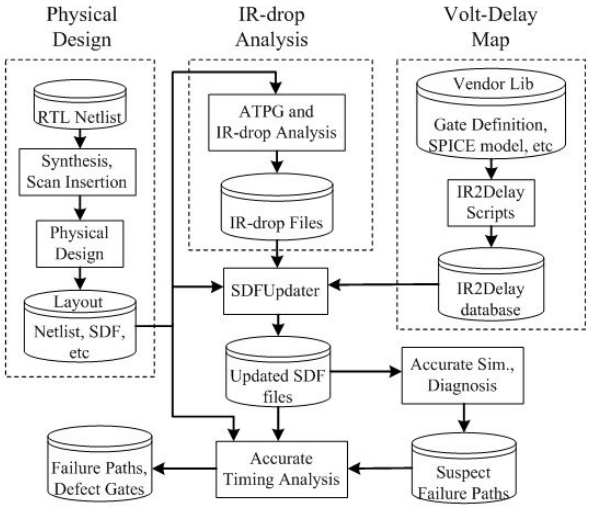


Figure 5. The flow for emulating and diagnosis IR-drop effects

As discussed in Section 4, we select an at-speed frequency based on the critical path delay to make sure that there are no failures with the original static SDF file when simulating the design. However, when we generate the dynamic SDF file for each pattern with IR-drop effect, and rerun simulation again with the same operating frequency, we can see some patterns fail with the dynamic SDF files. With the failure log, we can perform diagnosis to locate these defects. Therefore we can conclude that whether the failures are caused by IR drop or not.

In our experiments, 6 over total 203 patterns are failed with the selected frequency. However, with different guard banding frequency, the failed pattern number would change. Thus, our method could also be used for efficient guard banding selection against IR-drop failures during design validation.

Table 2. Profiles of sample gates in the ac97_ctrl benchmark

Instance / Model		U8701 / AND2X1		U8714 / NOR2X1		U12160 / INVX1
Power volt. (V)		1.59		1.61		1.76
path		A->Y	B->Y	A->Y	B->Y	A->Y
0->1 delay (ns)	original	0.0716	0.3208	0.0847	0.0693	0.0158
	updated	0.0845	0.3811	0.0946	0.0761	0.0166
	Incr.	18.0%	18.8%	11.7%	9.8%	5.1%
1->0 delay (ns)	original	0.0560	0.1256	0.0957	0.0873	0.0167
	updated	0.0661	0.1492	0.1068	0.0959	0.0165
	Incr.	18.0%	18.8%	11.6%	9.8%	-1.25%

Table 3. The timing of suspect failure paths for test pattern 28, based on IR-drop-aware dynamic SDF file (clock cycle: 7.63 ns)

Suspect path #	1	2	3	4
Path length (ns)	7.66	7.56	3.90	3.28

With the failure log of test patterns, as well as IR-drop-aware dynamic SDF files, we run diagnosis to report and do accurate timing analysis on the suspect failure paths. From the accurate timing analysis, it can be seen that not all the suspect paths violate the timing constrains, and should be eliminated from the IR-drop-caused failures. Take pattern 28 in the above experiment as an example, 4 suspect failure paths are reported and their path lengths based on our dynamic SDF are listed in Table 3. From this table it can be seen that only Path 1 is the real failure path. The other paths are not the real reason of the failed bit. Therefore, given that the design is failed by IR-drop, we can demonstrate exactly which paths caused these failures. Otherwise, just given the failure log, we can judge whether the failures are caused by IR drop or not.

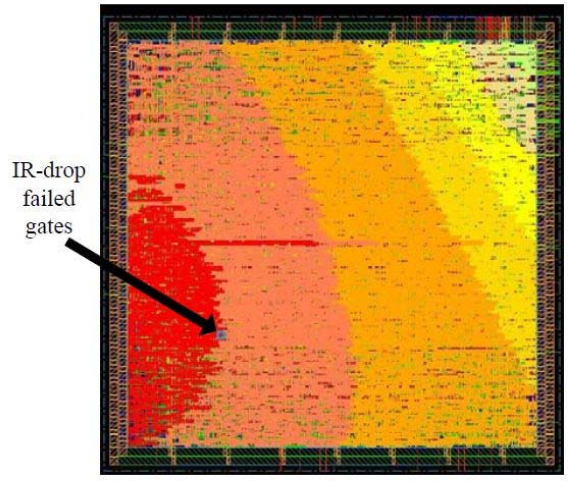


Figure 6. IR-drop plots and failed gates of a test pattern

Actually, it can be seen from the dynamic SDF file that only a couple of gates (two gates for the failure path in Table 3) experience severe IR-drop, and large delay

increase (about 20%) by applying and comparing the original static and updated dynamic SDFs to the failure paths. The delay increase of other gates is minor and negligible. In Figure 6, we pin-point the above gates with large delay increase in the layout and find that they are close to each other and both are located in the area suffers from severe IR-drop (the red part in the layout). In order to induce a comparable severe IR-drop in the small benchmark, only one pair of power/ground pins is placed at the top-right corner of the design.

The computation complexity of our dynamic SDF generation procedure is O(*nlogn*), where *n* is the number of logic gates in the design. Therefore, it is very fast and easy to scale to larger industry design. It has to be noted that the delay information in the SDF file may still not match the real silicon even all parasitic parameters are considered. However, with the silicon data, we can find a correlation between the SDF and real silicon delays. Thus we can scale our SDF to match real silicon delay. Furthermore, our IR-drop-induced extra delay is obtained from SPICE simulation with real parasitic consideration, which is much close to real silicon. Hence it can accurately reflect the IR-drop impact to real silicon.

6. Conclusions and Future Work

In this paper, we have presented an efficient IR-drop modeling and injection procedure for design performance evaluation. For each test pattern, the IR-drop analysis is performed to obtain its power voltage drop during the launch and capture cycles. SPICE simulation is performed to build up a database to map the power voltage drop of a gate to the delay increase with different output load capacitance. The static SDF file of the design is updated with IR-drop consideration and dynamic SDF files are generated for each pattern. It is a fast and accurate simulation flow that can be applied to large VLSI circuits. Based on the dynamic SDF files, we perform IR-drop related diagnosis, and improved the resolution of the current diagnosis tool.

With the dynamic pattern-dependent SDF files, we can perform many tasks at present and in future.

(1) Perform a more accurate simulation for performance evaluation of a design considering dynamic parametric variations caused by test patterns.

(2) Use dynamic SDF as constraints during ATPG to improve pattern quality.

(3) We will bring crosstalk effects to our procedure for dynamic SDF file generation and failure diagnosis and hopefully we can differentiate different root causes of at-speed pattern failures.

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