Memory Design

- Random Access Memory

Row decoder

n-1:k

k-1:0

n bit address

2^{m+k} memory cells wide

Column Decoder

Sense Amplifier

m bit data word
Memory Timing: Approaches

DRAM Timing
Multiplexed Addressing

SRAM Timing
Self-Timed

Address bus
Row Address
Column Address

RAS

CAS

Address Bus
Address transition initiates memory operation

RAS-CAS timing

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Memory Timing

- DRAM read cycle
  - Activate RAS, and place row address on bus
  - Row decoders select appropriate row
  - Activate CAS, and place column address on bus
  - Sense amps are activated and data is placed on the data bus
Memory Timing

from "Ars Technica RAM Guide", by Jon Stokes, ©Ars Technica LLC
Read-Only Memory Cells

Diode ROM

MOS ROM 1

MOS ROM 2
MOS OR ROM

V_{bias}
Pull-down loads

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MOS NOR ROM


Pull-up devices

V_{DD}

GND

GND

Pull-up devices
MOS NOR ROM Layout

Cell (9.5\(\lambda\) x 7\(\lambda\))

Programming using the Active Layer Only

- Polysilicon
- Metal1
- Diffusion
- Metal1 on Diffusion
MOS NOR ROM Layout

Cell (11\(\lambda\) x 7\(\lambda\))

Programming using the Contact Layer Only

- Polysilicon
- Metal1
- Diffusion
- Metal1 on Diffusion
MOS NAND ROM

All word lines high by default with exception of selected row
MOS NAND ROM Layout

Cell (8\(\lambda\) x 7\(\lambda\))

Programming using the Metal-1 Layer Only

No contact to VDD or GND necessary; drastically reduced cell size
Loss in performance compared to NOR ROM

- Polysilicon
- Diffusion
- Metal1 on Diffusion
Equivalent Transient Model for MOS NOR ROM

Model for NOR ROM

- Word line parasitics
  - Wire capacitance and gate capacitance
  - Wire resistance (polysilicon)

- Bit line parasitics
  - Resistance not dominant (metal)
  - Drain and Gate-Drain capacitance
Equivalent Transient Model for MOS NAND ROM

Model for NAND ROM

- Word line parasitics
  - Similar to NOR ROM
- Bit line parasitics
  - Resistance of cascaded transistors dominates
  - Drain/Source and complete gate capacitance
Decreasing Word Line Delay

(a) Driving the word line from both sides

(b) Using a metal bypass

(c) Use silicides
Precharged MOS NOR ROM

PMOS precharge device can be made as large as necessary, but clock driver becomes harder to design.
Non-Volatile Memories

The Floating-gate transistor (FAMOS)

Device cross-section

Schematic symbol
Floating-Gate Transistor Programming

Avalanche injection

Removing programming voltage leaves charge trapped

Programming results in higher $V_T$. 
FLOTOX EEPROM

Floating gate
Source

20–30 nm

Substrate
10 nm

Gate
Drain

\( n^1 \)

\( n^1 \)

\( p \)

FLOTOX transistor

Fowler-Nordheim
I-V characteristic

\[ I \]

\[ V_{GD} \]

-10 V

10 V
Absolute threshold control is hard
Unprogrammed transistor might be depletion
⇒ 2 transistor cell
Flash EEPROM

Control gate

Floating gate

Thin tunneling oxide

 erased

programming

p-substrate

n⁺ source

n⁺ drain

Many other options …
Cross-sections of NVM cells

Flash
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Courtesy Intel

EPROM
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Basic Operations in a NOR Flash Memory

Erase
Basic Operations in a NOR Flash Memory
Write

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Basic Operations in a NOR Flash Memory
Read

![Diagram of NOR Flash Memory]

- 5 V
- 0 V
- 1 V
Memory Design

• Register File
  – RAM with multiple read or write ports
  – You can read or write multiple data values at the same time
  – Useful in data processing applications
Memory Design

- Register File Cell

```
<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>RB1</td>
<td></td>
<td></td>
<td>RB1</td>
</tr>
<tr>
<td>RB0</td>
<td></td>
<td></td>
<td>RB0</td>
</tr>
</tbody>
</table>

Word select 0
Word select 1
Write enable
Write data
```
Memory Design

• Content Addressable Memory (CAM)
  – Instead of finding memory by address, find it by content
  – Search or match every single word in memory array
Static CAM Memory Cell

Wired-NOR Match Line
CAM in Cache Memory

- **CAM ARRAY**
- **Input Drivers**
- **Tag**
- **Hit**
- **R/W**
- **Sense Amps / Input Drivers**
- **SRAM ARRAY**
- **Data**
- **Address**
Memory Design

• Other memory structures
  – FIFOs
  – LIFOs
  – SIPOs
Periphery

- Decoders
- Sense Amplifiers
- Input/Output Buffers
- Control / Timing Circuitry
Memory Design

• Row decoder
Memory Design

• Row decoder
  – With multiple inputs (>4), two problems
    • Speed of gates becomes a problem
      – Use hierarchy of NANDS/NORS
      – Use predecoding - decode upper bits first and use lower bits to select from there
    • Increased fanout
      – Use minimum sized input gates
Hierarchical Decoders

Multi-stage implementation improves performance

NAND decoder using 2-input pre-decoders
Dynamic Decoders

2-input NOR decoder

2-input NAND decoder
Memory Design

- Column decoder

A1  A0

Memory Cells

Data Out
Memory Design

• Column decoder
Memory Design

• Column decoder
  – AND-decoder based
    • On the order of $N \cdot 2^N$ transistors
  – Binary tree based
    • Slow because of the series of pass-transistors
  – Usually use a combination of the two
Memory Design

- **Sense Amplifier**
  - Time to get through row decoder, column pull-down and column decoder can be very long
  - Use a sense amplifier to speed it up
    - Sense small differences in voltage and amplify it to rail voltage
    - Can be differential or single-ended
    - Usually use transistors with high threshold voltages
Sense Amplifiers

\[ t_p = \frac{C \cdot \Delta V}{I_{av}} \]

\[ \text{large} \rightarrow \text{small} \]

Idea: Use Sense Amplifier

\[ \Delta V \text{ as small as possible} \]
Differential Sense Amplifier

Directly applicable to SRAMs
Next class

• Memory Reliability and Yield
• Control logic